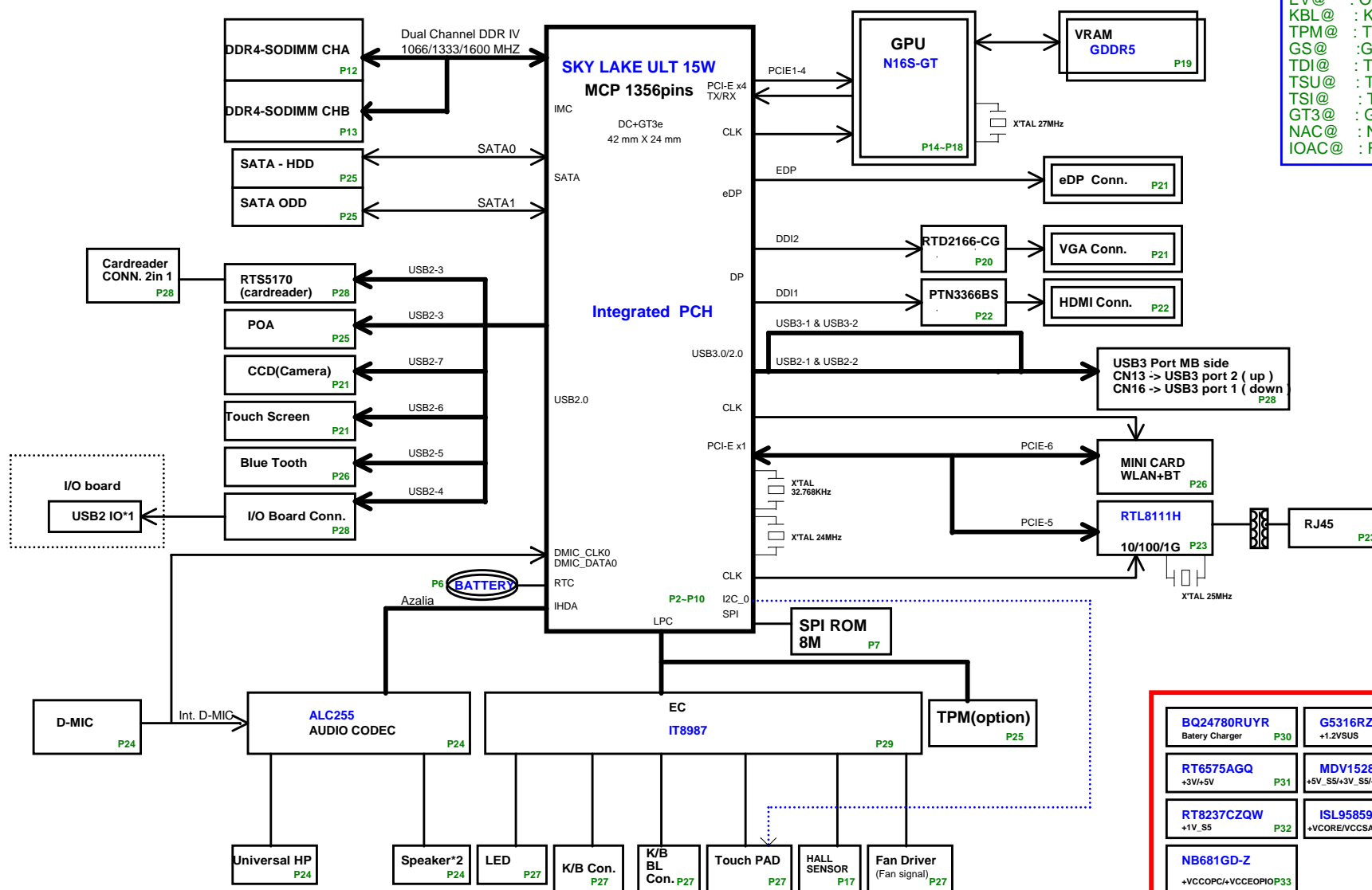


Z8V Serials SKL ULT SYSTEM BLOCK DIAGRAM

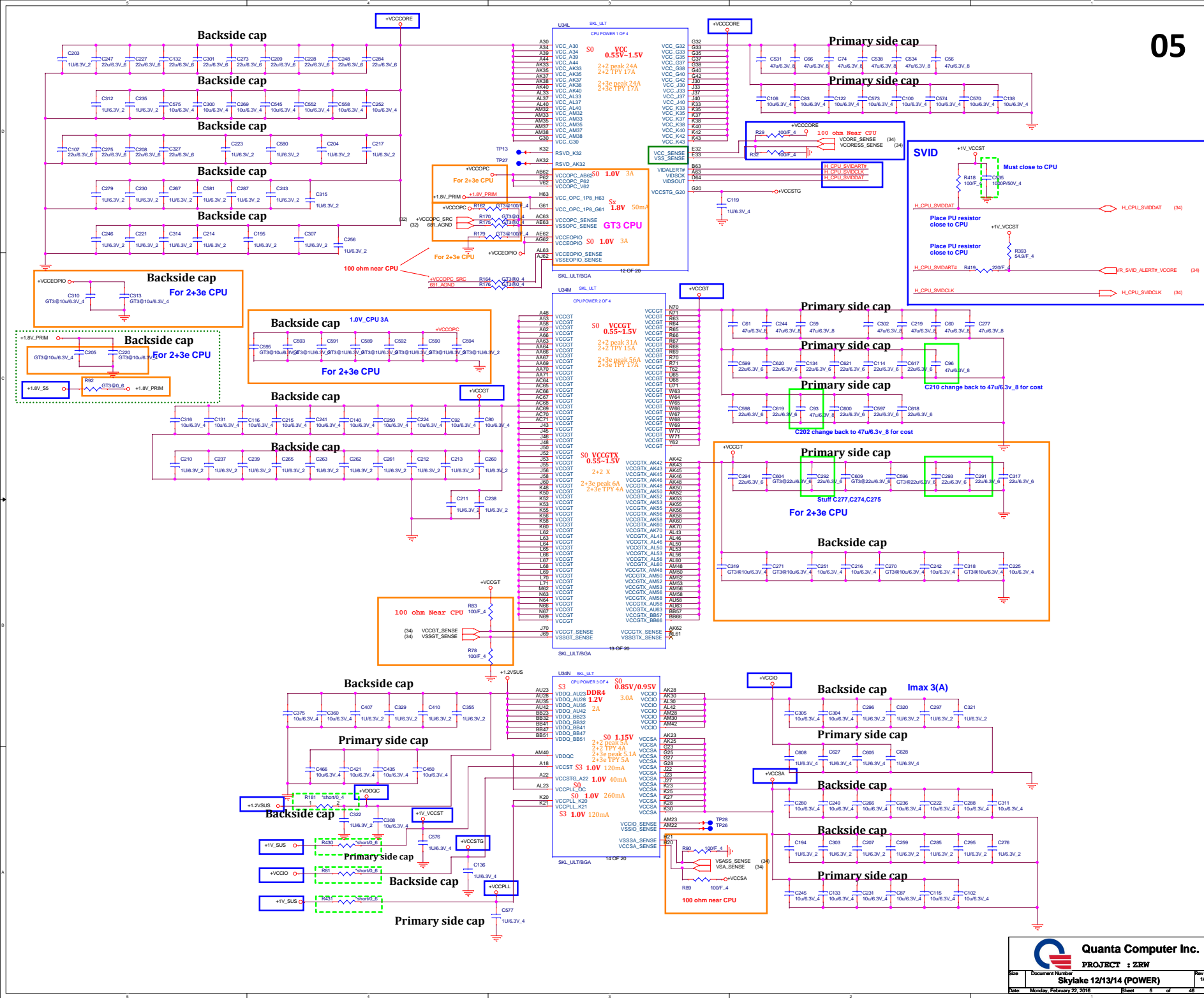


BOM

- IV@ : iGPU
- EV@ : Optimus
- KBL@ : Keyboard backlight
- TPM@ : TPM
- GS@ : G-SENSOR
- TDI@ : TOUCH PAD I2C
- TSU@ : TOUCH SCREEN USB
- TSI@ : TOUCH SCREEN I2C
- GT3@ : GT3 CPU
- NAC@ : Non IOAC
- IOAC@ : For IOAC

BQ24780RUYR Battery Charger P30	G5316RZ1D +1.2VSUS P34	Thermal Protection Discharger P38
RT6575AGQ +3V/+5V P31	MDV1528Q +5V_SS/+3V_SS/+3V/+5V P31	UP1658RQKF +VGPU_CORE P39
RT8237CZQW +1V_SS P32	ISL95859HRTZ-T +VCORE/VCCSA/VCCGT P35	RT8068AZQW +1.05V_GFX/+3V_GFX +1.5V_GFX P40
NB681GD-Z +VCCOPC/+VCCOPIO P33		

Size	Document Number	Rev
	Skylake 6/7 (PEG/DMI/FDI)	1A
Date:	Monday, February 22, 2016	Sheet 4 of 46



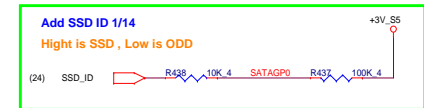
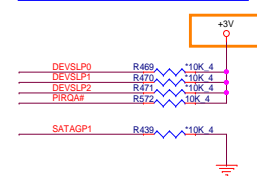
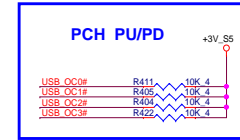
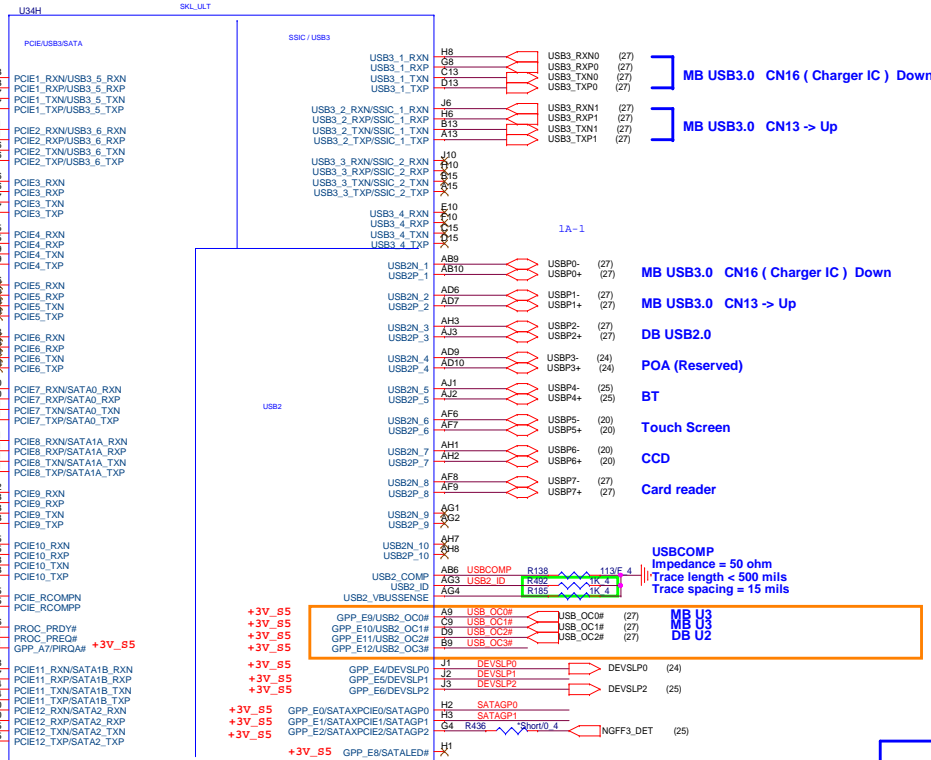
dGPU PEG#4

LAN

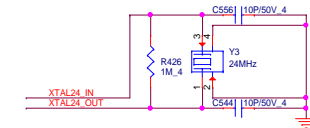
WIFI

HDD

ODD



Skylake-U used 24 MHz (50 Ohm ESR) XTAL

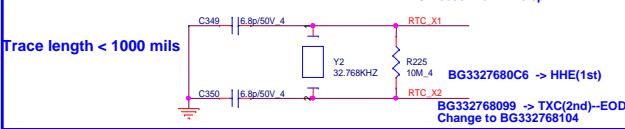


BG624000078 -> HHE(1st)

BG624000044 -> TXC(2nd)

Note: Change Y4 to 38.4 MHz(ESR 30 ohm) for Cannonlake U

RTC Clock 32.768KHz (RTC)

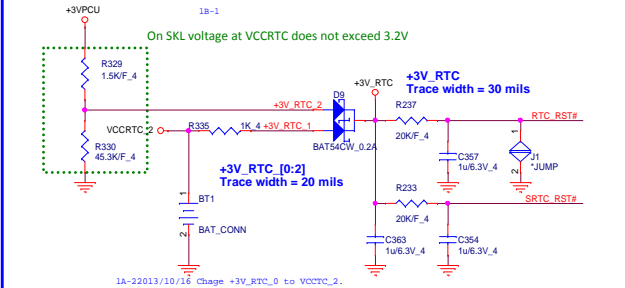


CH01006JB08 -> 10p

CH01506JB06 -> 15p

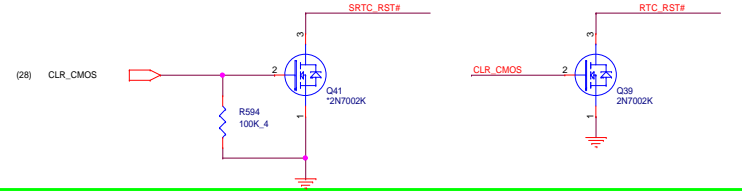
CH-6806TB01 -> 6.8p

RTC Circuitry (RTC)



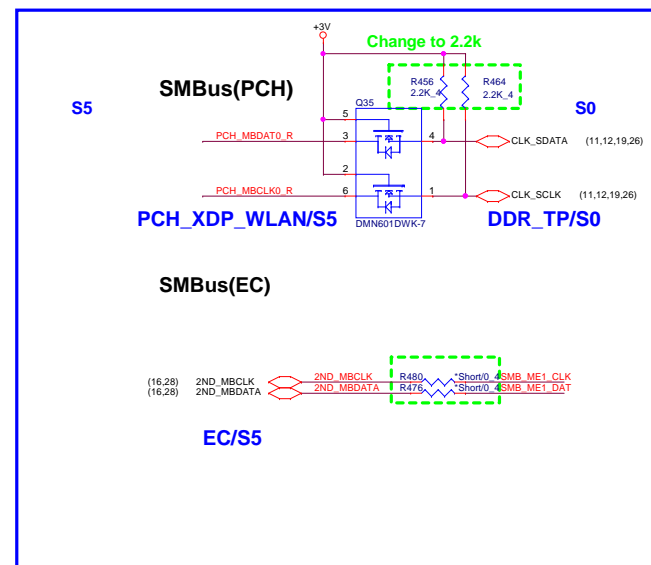
1. A0H03003057 DBV CR2032
2. A0H03003003 VDE CR2032

add for EC reset RTC



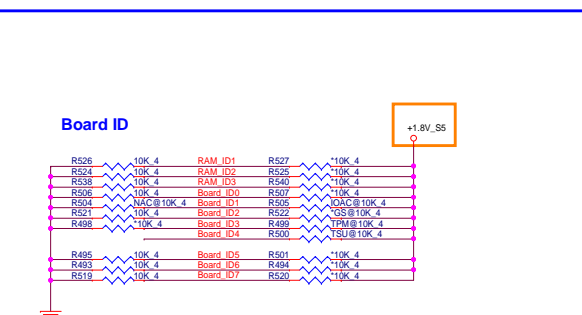
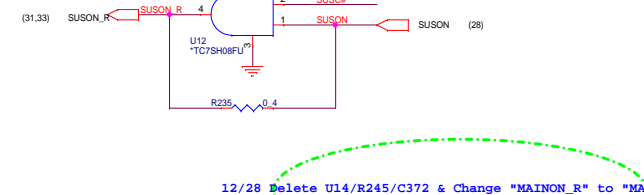
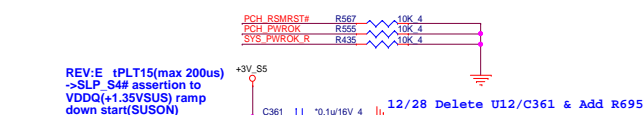
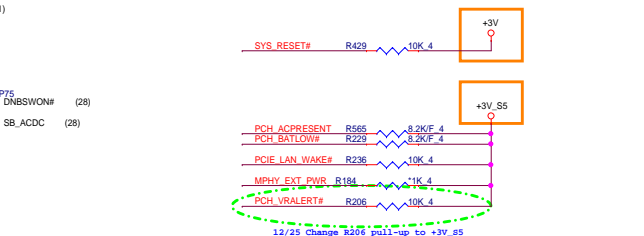
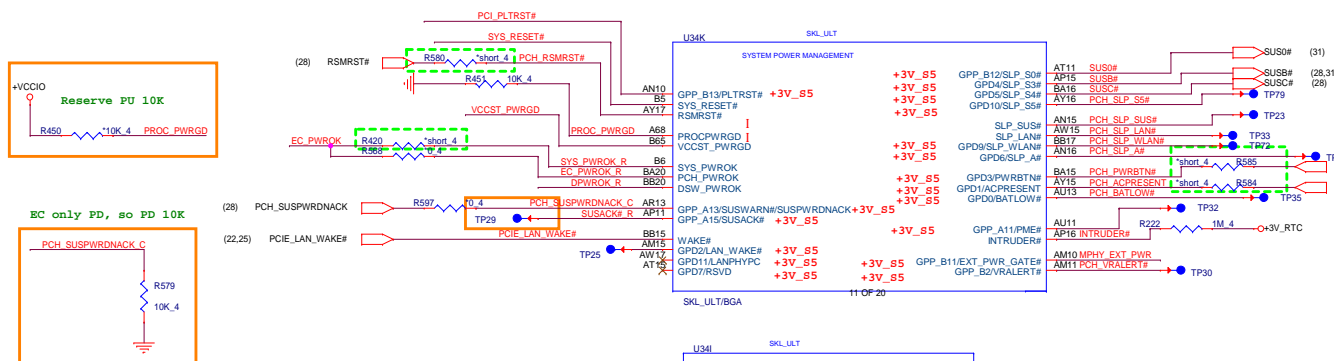
1V power plane

0.71 checklist p14

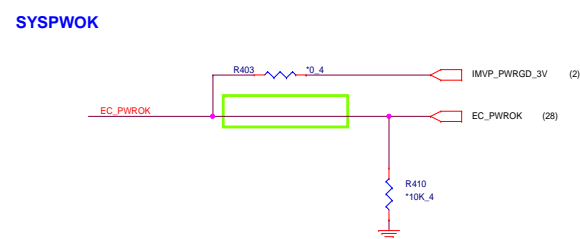
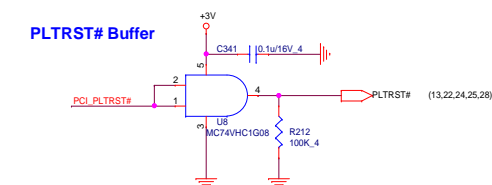
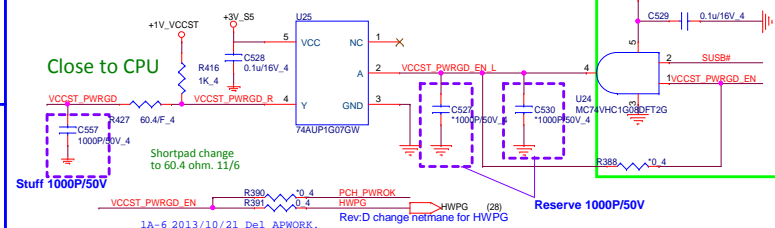
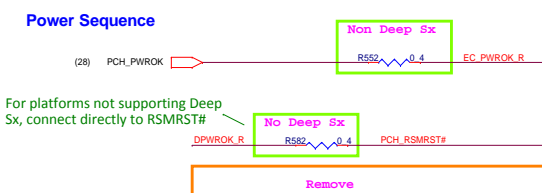
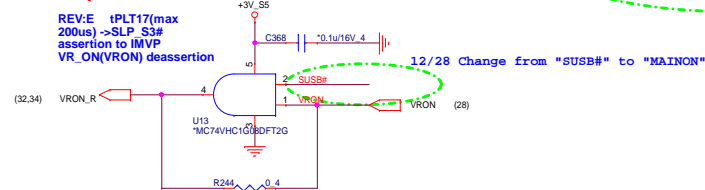
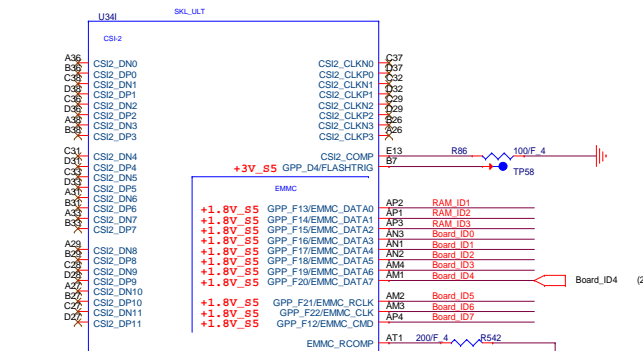


SP@ socket P/N: DFHS08FS023 only for A-TEST

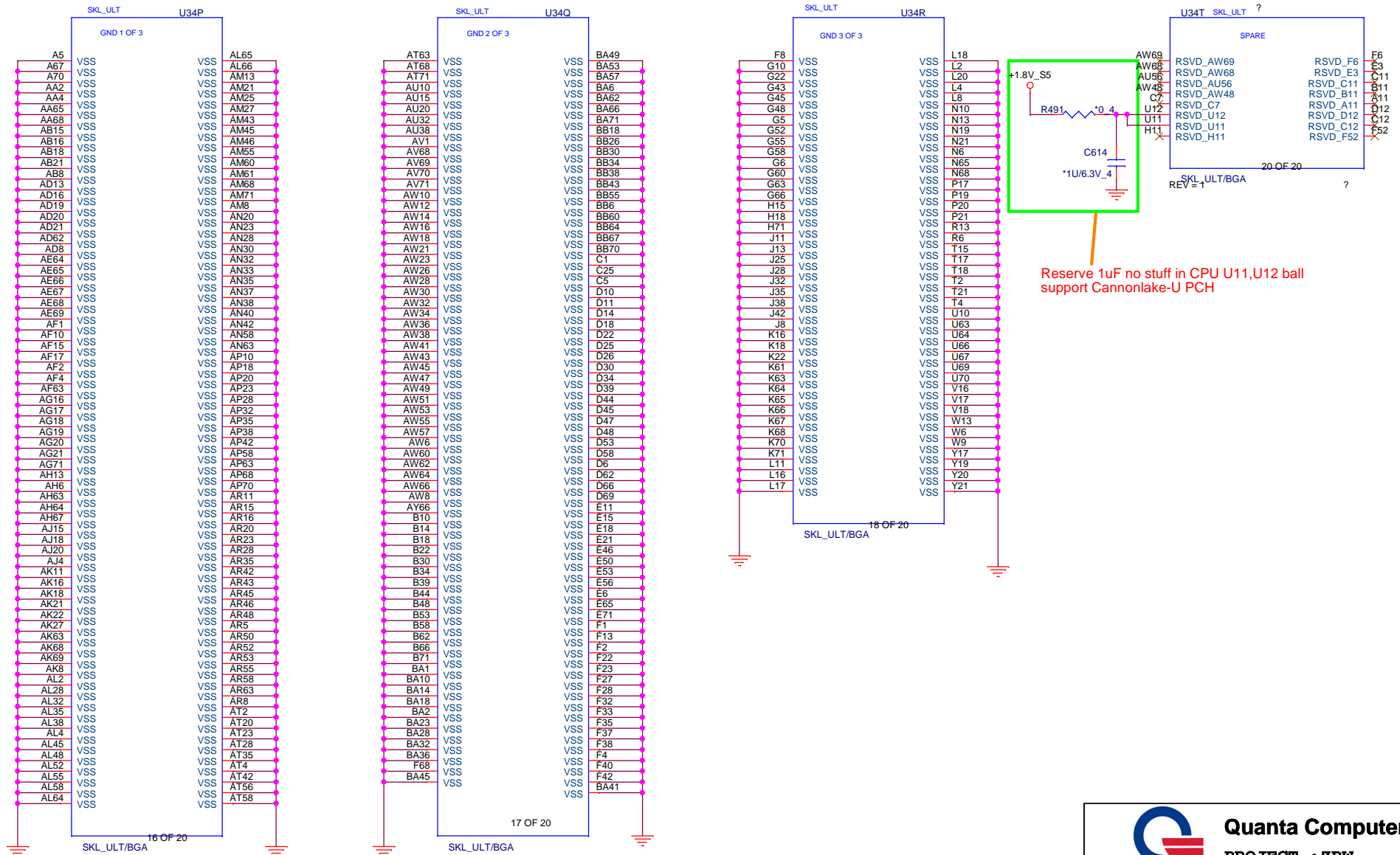
SPI ROM	Vender	Size	Quanta P/N	Vender P/N
Skylake 3.3V	WND	8M	AKE3EFF0N07	W25Q64FVSSIQ
	GGD	8M	AKE2EZ2N0Q00	GD25B64CSIGR



	Low	High
BOARD_ID0	VRAM X32 (R506)	VRAM X16 (R507)
BOARD_ID1	Non IOAC (R504)	IOAC (R505)
BOARD_ID2	Non G-sensor (R521)	G-sensor (R522)
BOARD_ID3	No TPM (R498)	TPM (R499)
BOARD_ID4	No-Touch panel	Touch panel (R500)

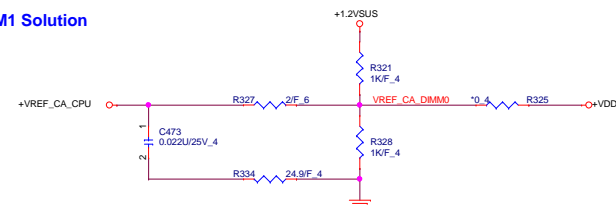


Skylake ULT (GND)



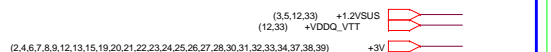
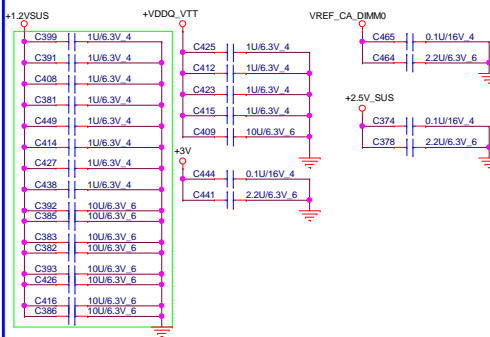


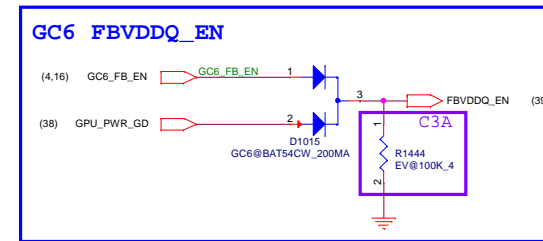
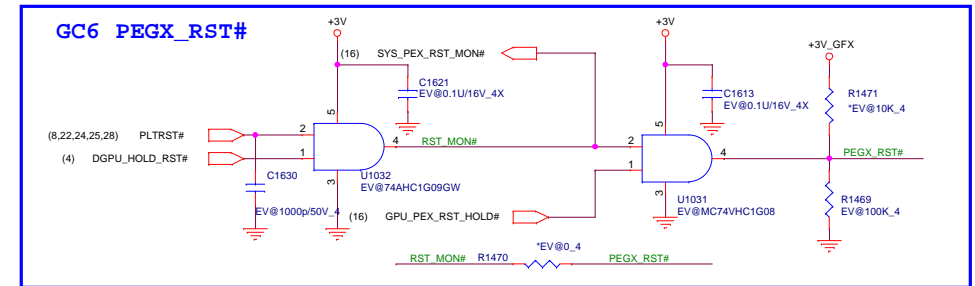
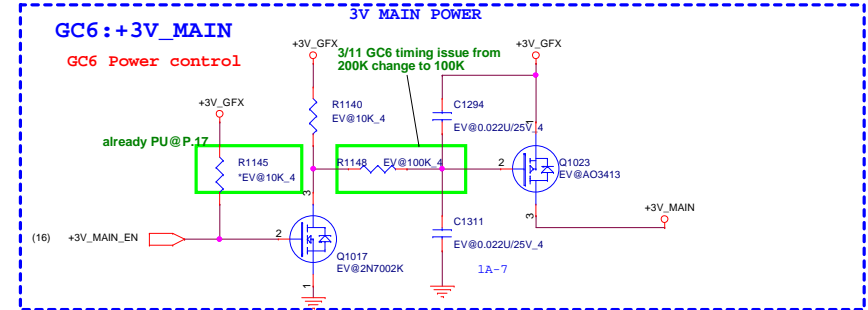
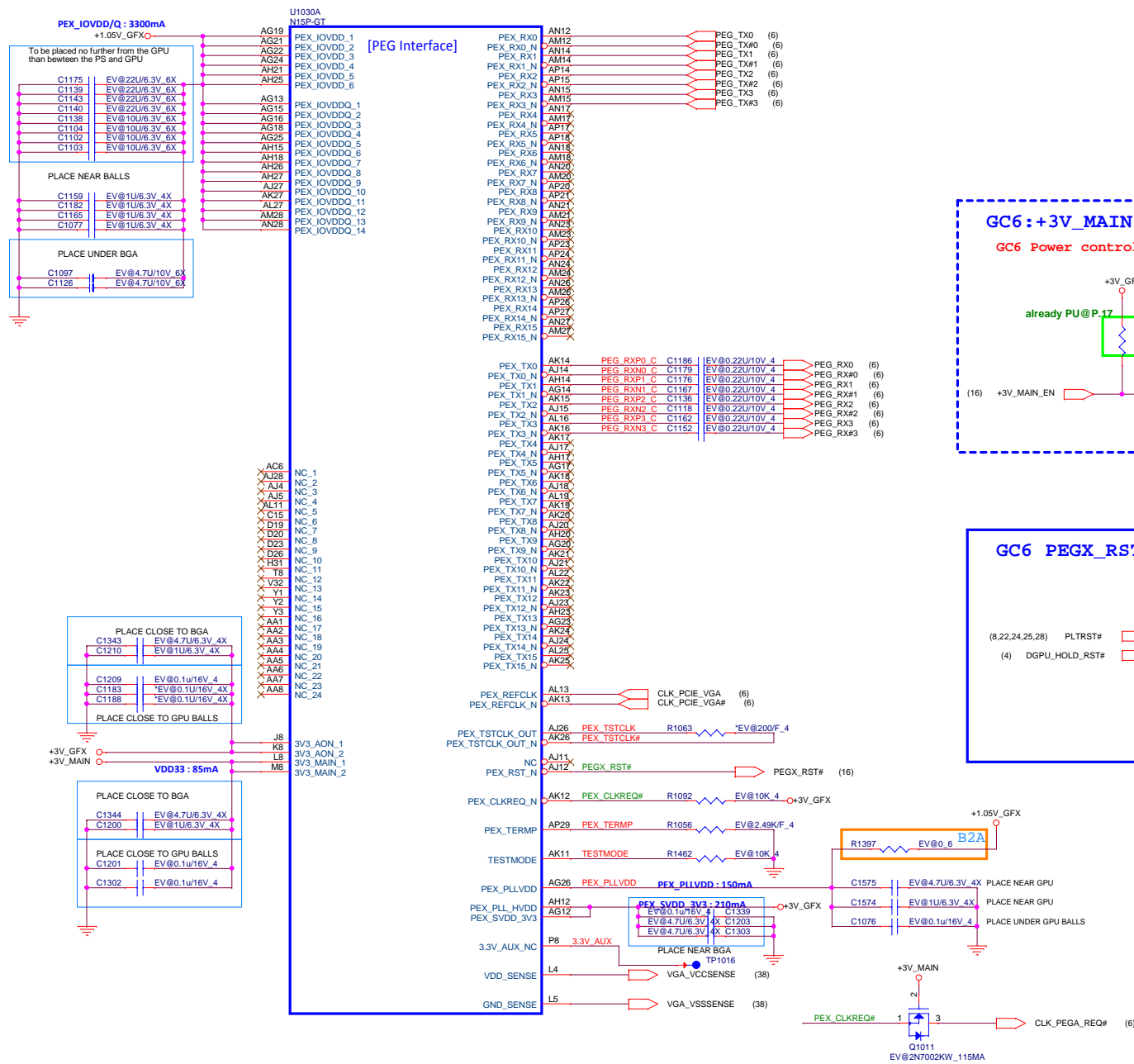
VREF DQ0 M1 Solution

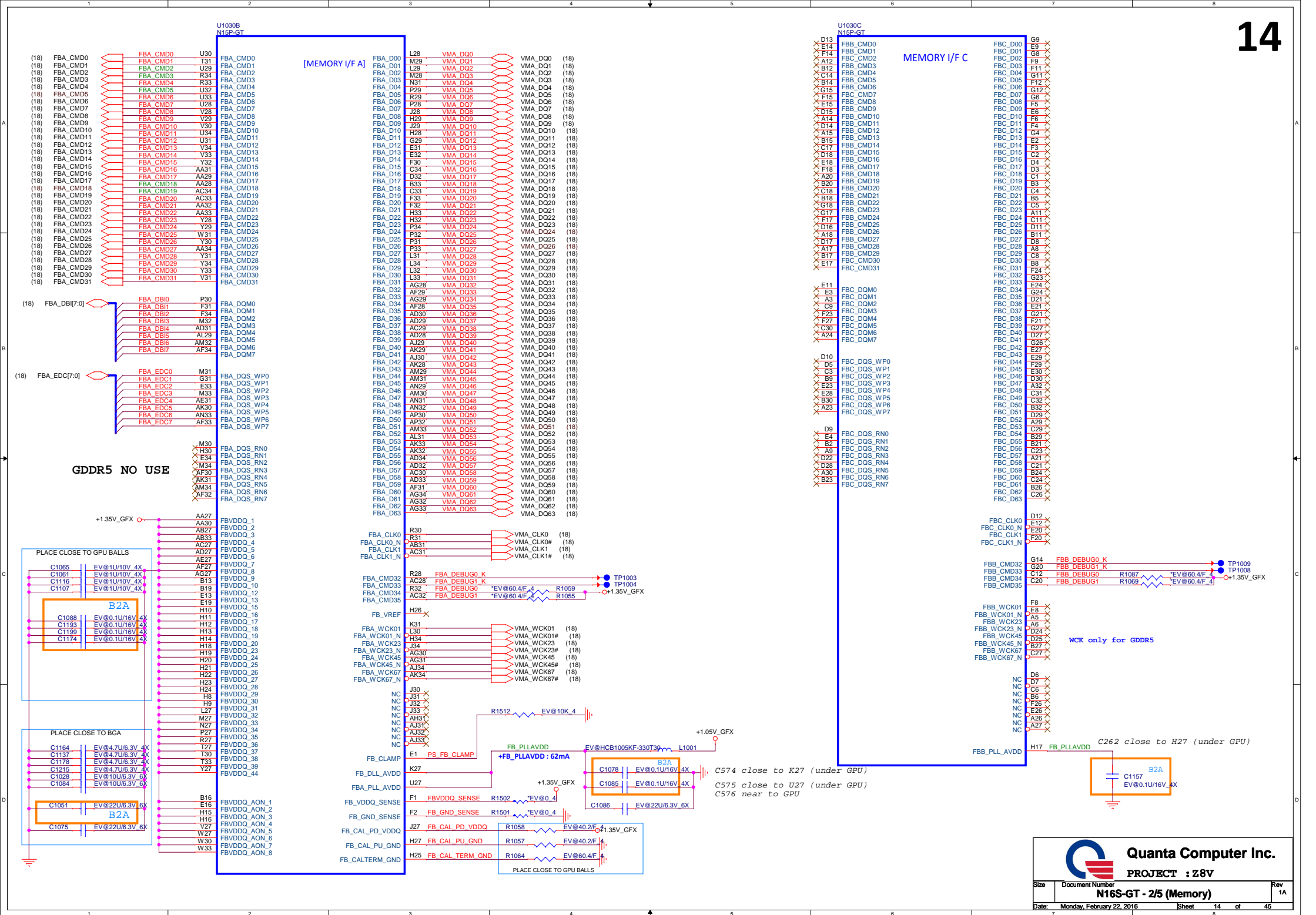


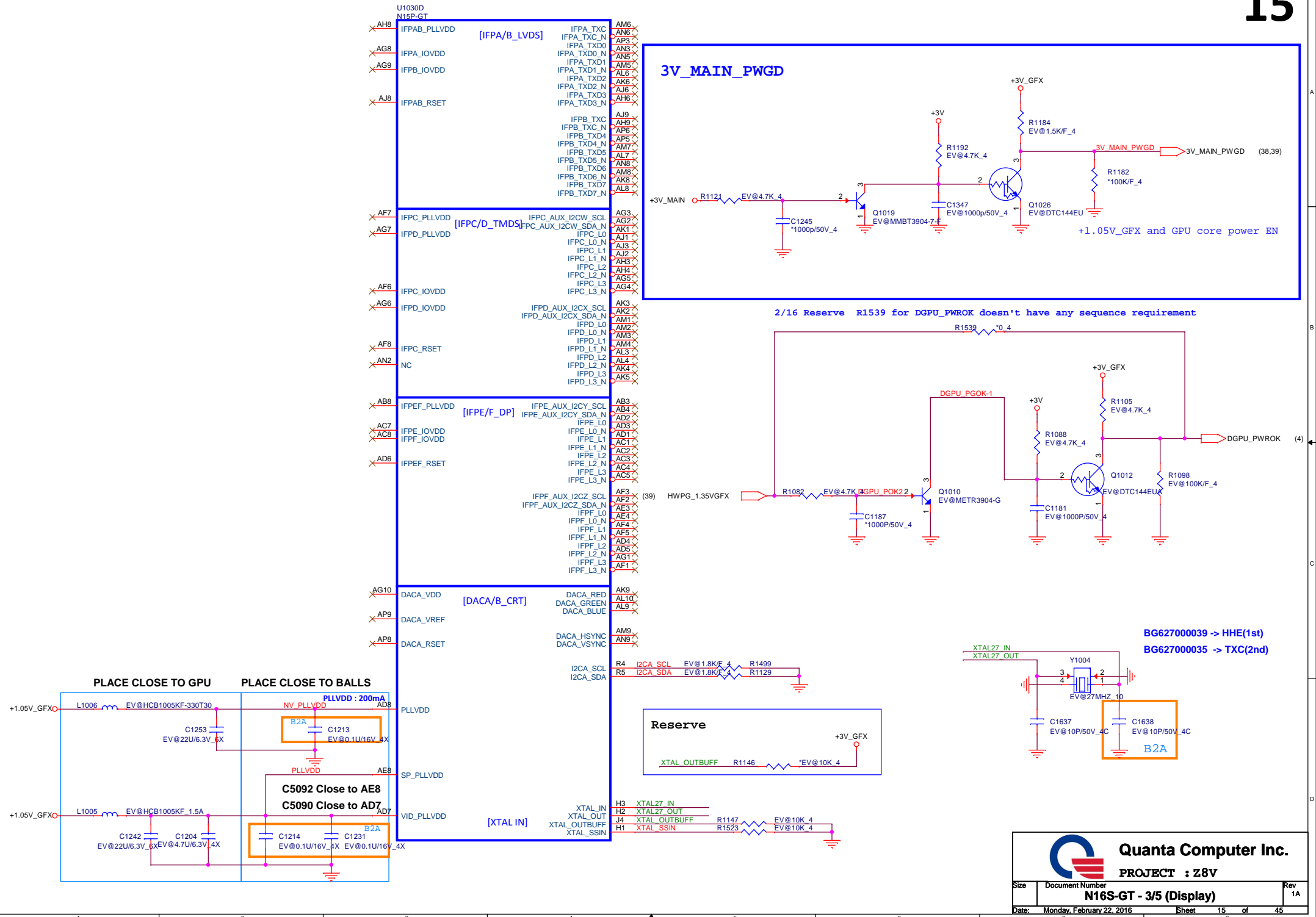
Place these Caps near So-Dimm1.

1uF/10uF 4pcs on each side of connector







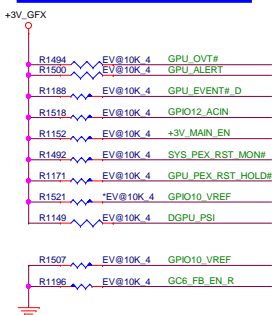


Resistor P/N
 4.99K → CS24992FB26
 10K → CS31002FB26
 15K → CS31502FB24
 20K → CS32002FB29
 24.9K → CS32492FB16
 30.1K → CS33012FB18
 34.8K → CS3482FB22
 45.3K → CS34532FB18 GM
 49.9K → CS34992FB10 GT

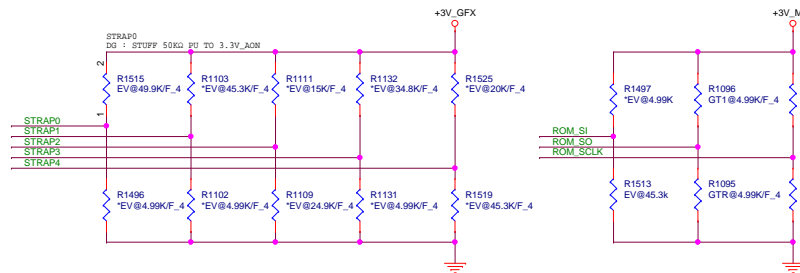
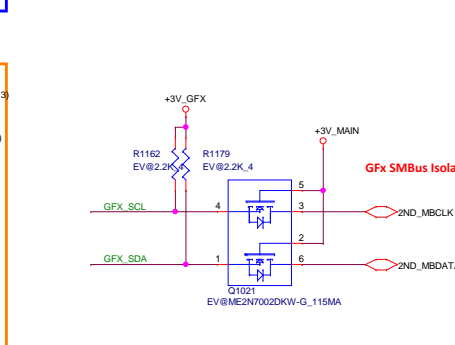
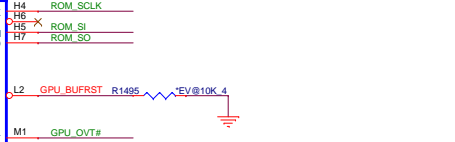
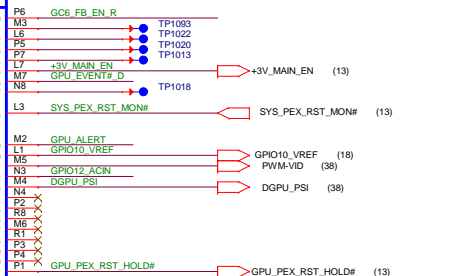
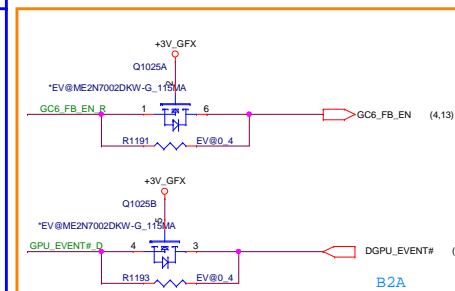
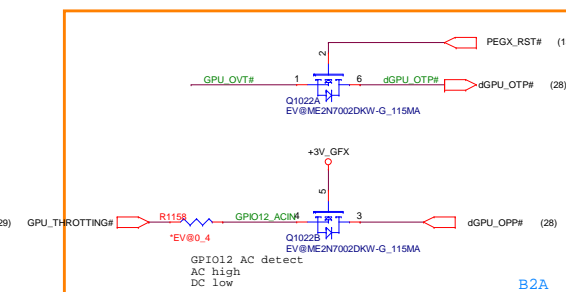
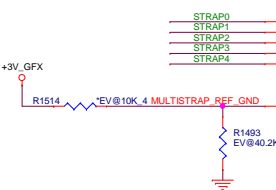
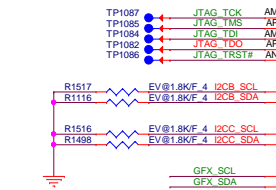
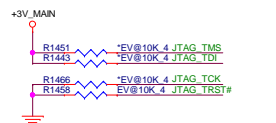
U1030E
 N16S-GT

[MIOA]

[MIOB]



Reserve PU/PD for Debug



	PU +3V_MAIN	PD
4.99K	1000	0000
10K	1001	0001
15K	1010	0010
20K	1011	0011
24.9K	1100	0100
30.1K	1101	0101
34.8K	1110	0110
45.3K	1111	0111

Mutil-level mode strapping:

For N16S-GT1-KB-A2 :
 R490=40.2K PD
 1.ROM_SCLK = 4.99K PU
 2.ROM_SO = 4.99K PU (N16S-GTR = 4.99KPD)
 3.ROM_SI = Memory strap setting
 4.STRAP0 = 49.9k PU
 5.Strap4~1 = Reserve Pull up and Pull down

	N16S-GT1-KB-A2	N16S-GTR
ROM_SO	R93 PU 4.99K	R92 PD 4.99K
ROM_SI	As below configuration table	

N16S-GT1-KB-A2 VRAM Configuration Table:

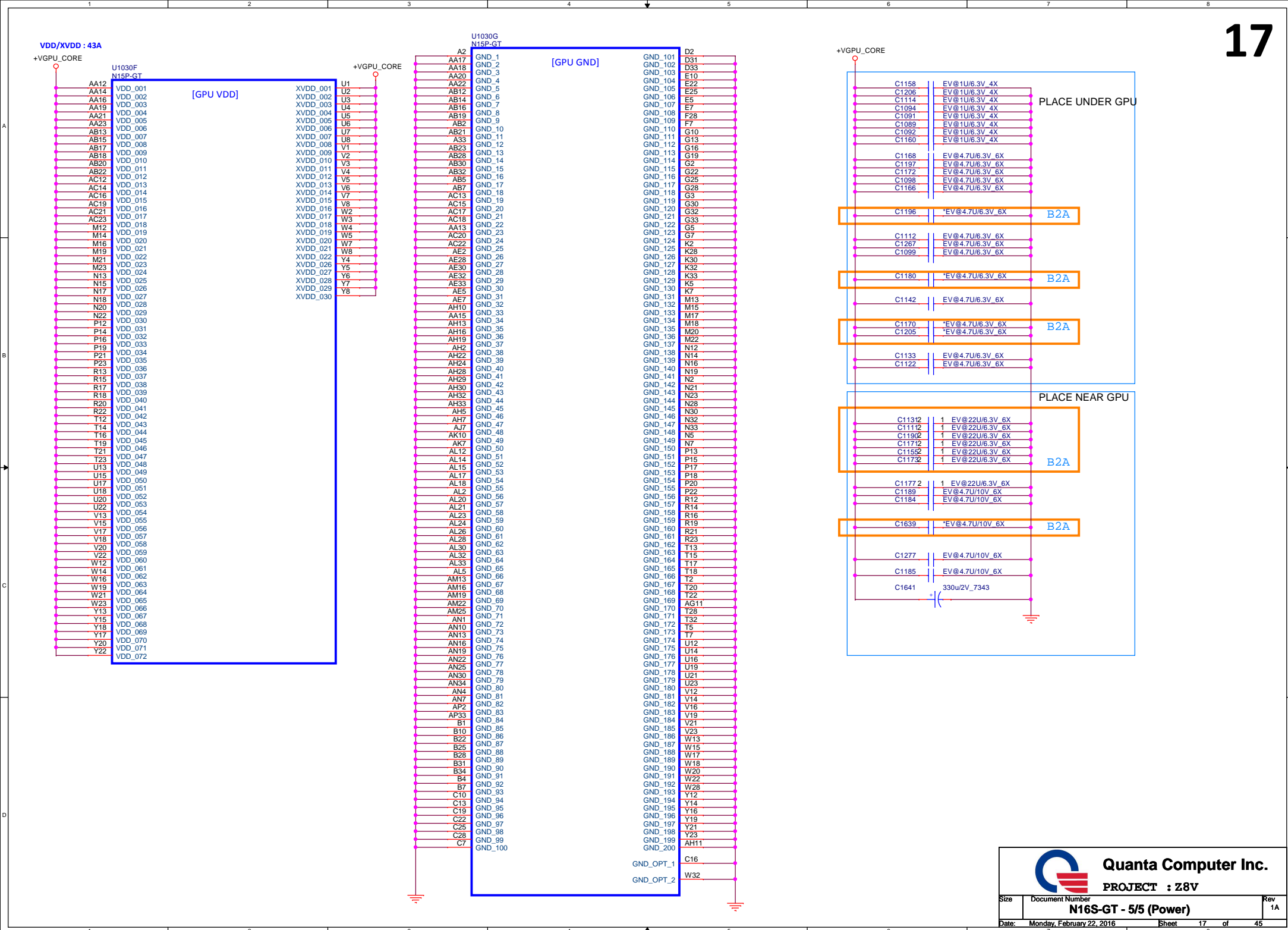
	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx32,2500MHz GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDTS02 AKG5LGUTL04	4.99K Pull up 10K Pull up
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDTS02 AKG5LGUTL04	4.99K Pull up 10K Pull up

N16S-GTR VRAM Configuration Table:

	ROM_SI	DESCRIPTION	Vendor	Vendor P/N	STN P/N	ROM_SI
4GbX2 (1GB)	0011 (0x3) 0110 (0x6)	GDDR5 128MBx32,2500MHz GDDR5 128MBx32,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
4GbX4 (2GB)	0011 (0x3) 0110 (0x6)	GDDR5 256MBx16,2500MHz GDDR5 256MBx16,2500MHz	SAMSUNG HYNIX	K4G41325FC-HC03 --C die H5GC4H24AJR-T2C --A die	AKG5PGDT505 AKG5PWUTW21	20K Pull down 34.8K Pull down
8GbX2 (2GB)	0000 (0x0) 0001 (0x1)	GDDR5 256MBx32,2500MHz GDDR5 256MBx32,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDTS02 AKG5LGUTL04	4.99K Pull down 10K Pull down
8GbX4 (4GB)	0000 (0x0) 0001 (0x1)	GDDR5 512MBx16,2500MHz GDDR5 512MBx16,2500MHz	SAMSUNG MICRON	K4G80325FB-HC03 --B die MT51J256M32HF-60:A--A die	AKG5QGDTS02 AKG5LGUTL04	4.99K Pull down 10K Pull down

N16S-GT1-KB-A2 (GB4b-128)

	Logical Strapping Bit3	Logical Strapping Bit2	Logical Strapping Bit1	Logical Strapping Bit0	
ROM_SCLK	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED	0000
ROM_SI	RAMCFG[3]	RAMCFG[2]	RAMCFG[1]	RAMCFG[0]	XXXX
ROM_SO	DEVID_SEL	PCIE_CFG	SMB_ALT_ADDR	VGA_DEVICE	0000
STRAP0	Keep footprint to PU to 3V3_AON and PD to GND [Stuff 49.9K PU]				0001
STRAP1	Keep footprint to PU to 3V3_AON and PD to GND [Do Not Stuff]				
STRAP2					
STRAP3					
STRAP4					



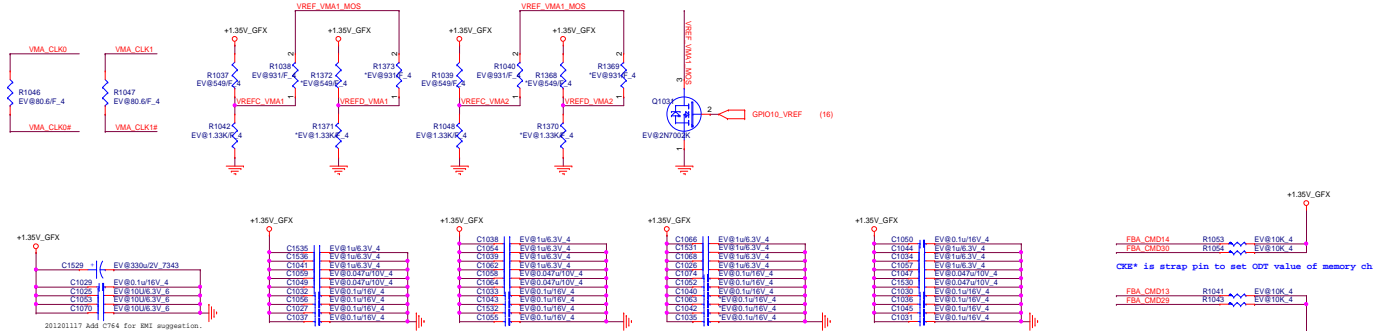
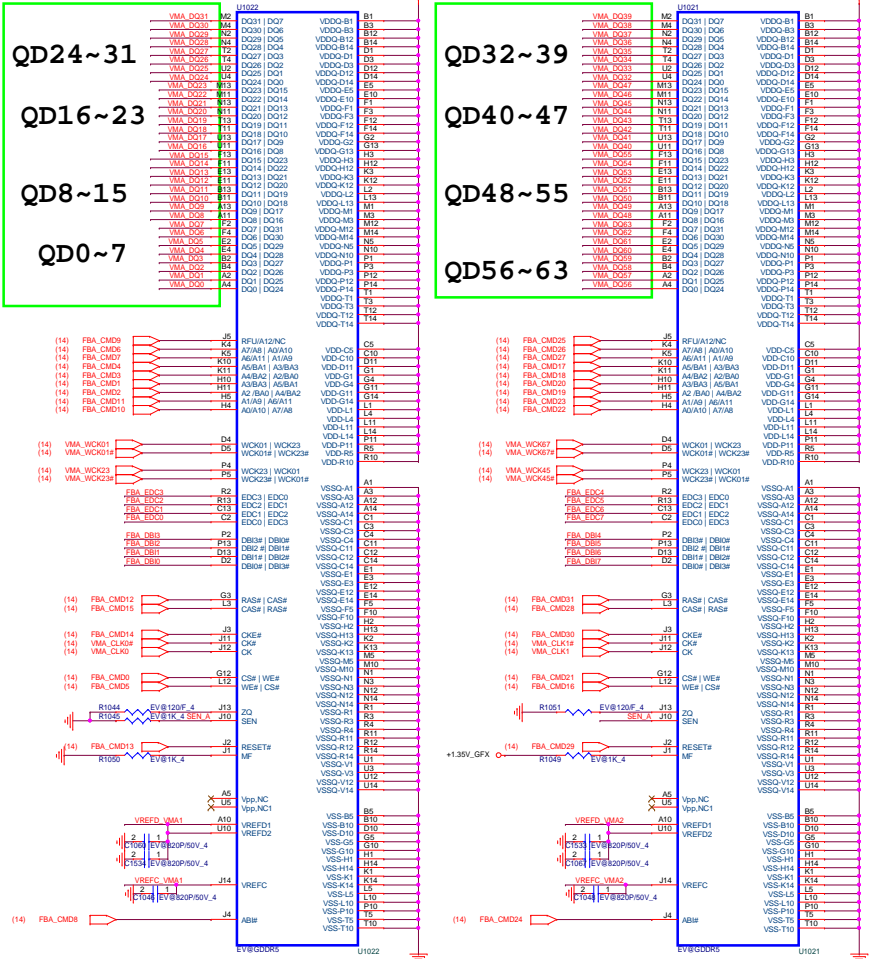
Channel 0
<0-31>

LOWER HALF

Channel 0
<32-63>

MF=0 Non-mirrored

MF=1 mirrored



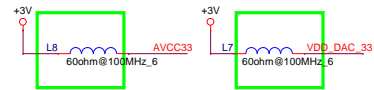
GDDR5 Mode II Mapping

Channel	Bank	Memory
0	0	0
0	1	1
0	2	2
0	3	3
0	4	4
0	5	5
0	6	6
0	7	7
0	8	8
0	9	9
0	10	10
0	11	11
0	12	12
0	13	13
0	14	14
0	15	15
0	16	16
0	17	17
0	18	18
0	19	19
0	20	20
0	21	21
0	22	22
0	23	23
0	24	24
0	25	25
0	26	26
0	27	27
0	28	28
0	29	29
0	30	30
0	31	31

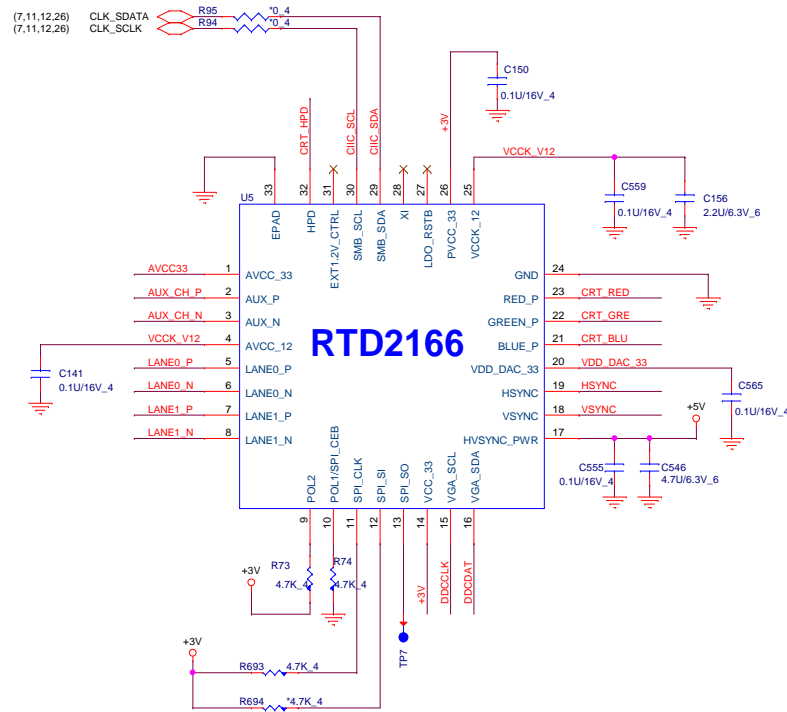
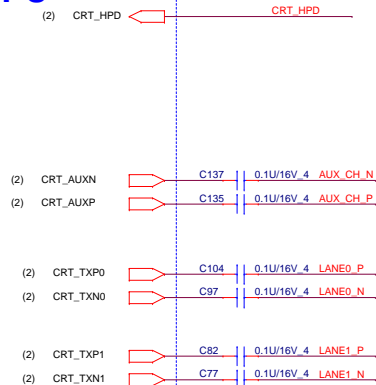
RST PD place @ the end of daisy-chain.

DP TO VGA

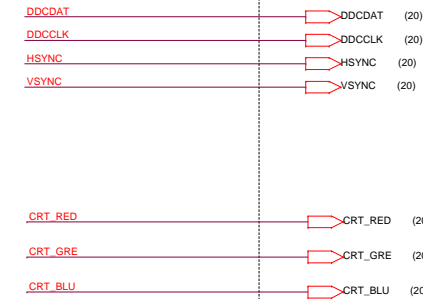
Power



CPU



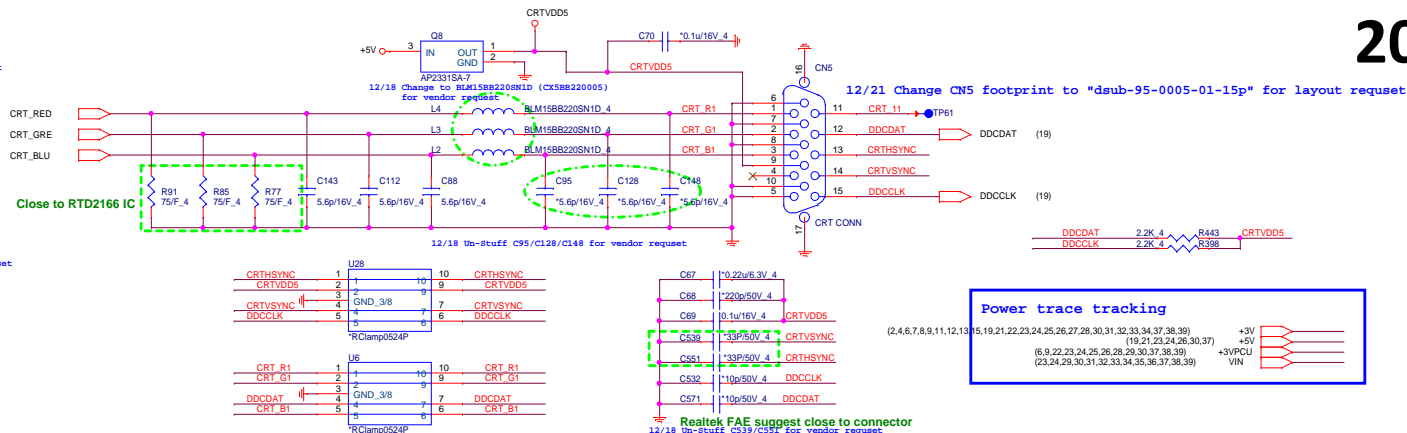
VGA



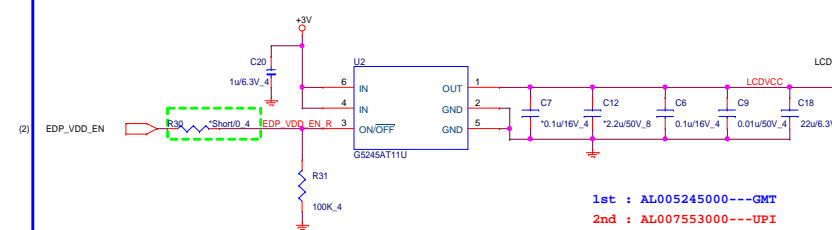
Note:

- 1- C1,C3,C4,C5,C11,C16, C21 should be placed close to chip
- 2- C5 should be X5R material
- 3- R6, R7, R8 should be 75 ohm with +/-1%
- 4- Suggest to connect Pin 29 and Pin 30 to PCH SMBUS for debug purpose.
- 5- This configuration is for internal ROM mode and using embedded LDO mode.

(2,4,6,7,8,9,11,12,13,15,20,21,22,23,24,25,26,27,28,30,31,32,33,34,37,38,39) +3V
(20,21,23,24,26,30,37) +5V



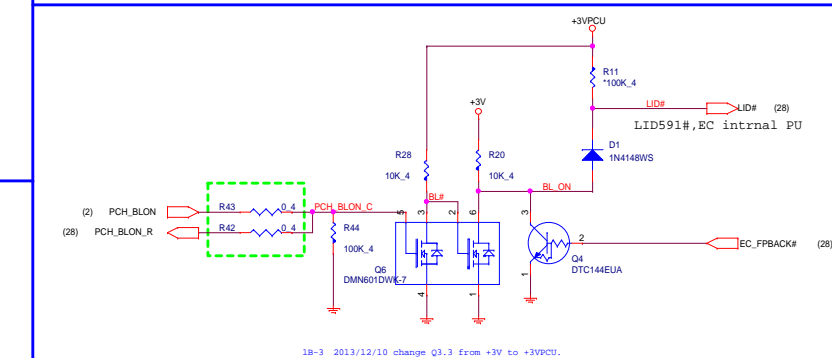
LCD Power



S0

TPD->100kHz, TS=400kHz
 Intel design guide suggestion
 MCP PIN 10u.
 Per inch 3u TS=3x5inch
 400kHz10-100u =2.4-0.4k.
 100kHz 10-100u=9k-1k.

1st:AL009249000 -- BCD
2nd:AL009132001 -- ANC

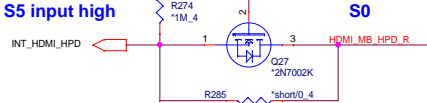


HDMI <HDM>

OE_N	DDC_EN	HPD_SINK	Source output	PTN3366 power mode
LOW	HIGH	HIGH	source active	Active mode; DDC active
LOW	LOW	LOW	don't care	Standby mode
HIGH	LOW	don't care	don't care	Ultra low-power mode

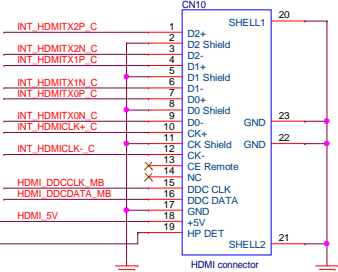
From PCH

HDMI-detect

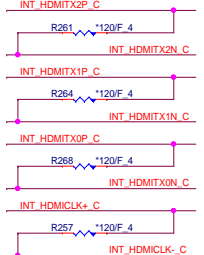


DDS AL002331000

HDMI connector

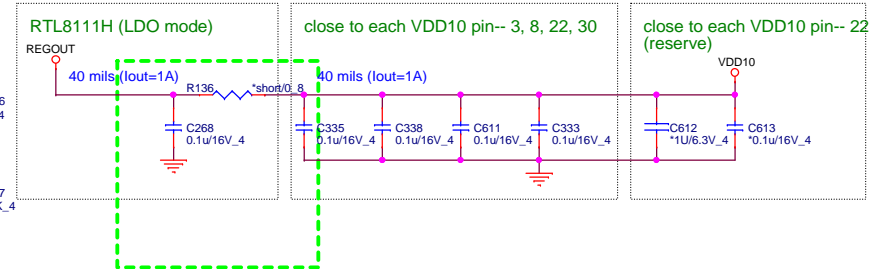
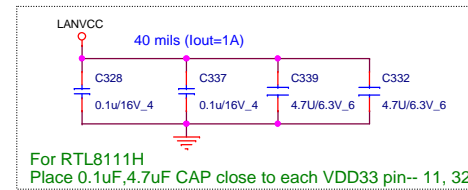
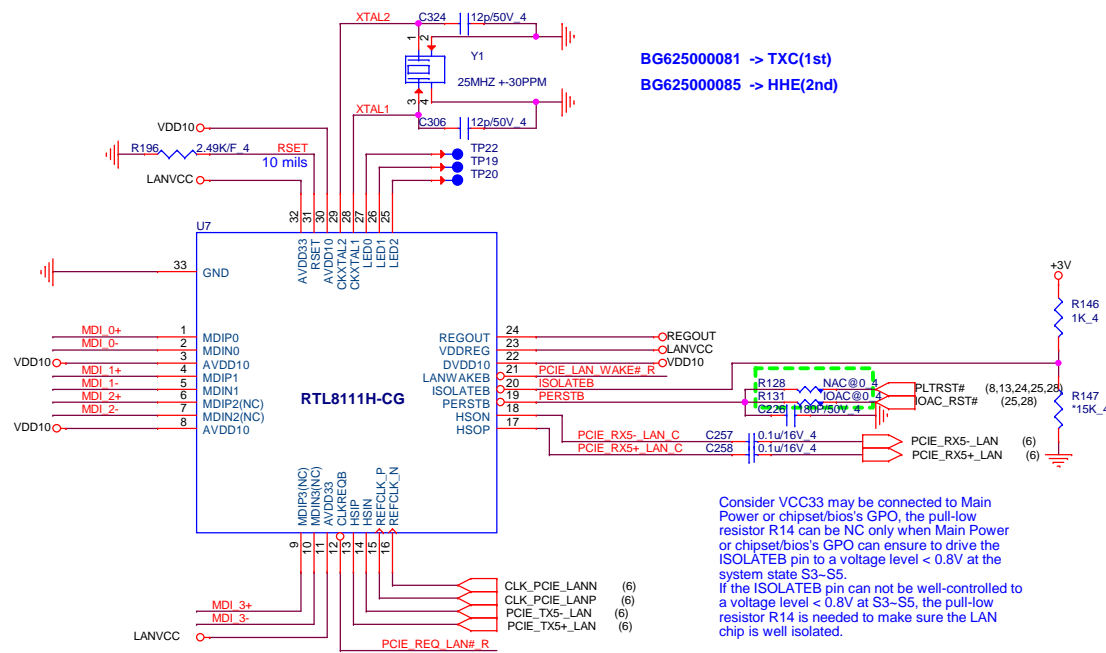


EMI

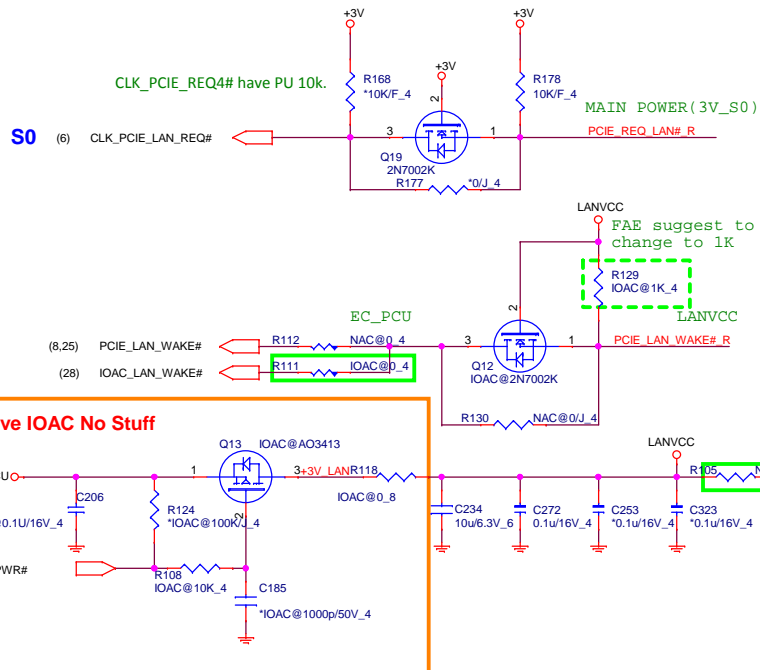


Power trace tracking

(2,4,6,7,8,9,11,12,13,15,19,20,22,23,24,25,26,27,28,30,31,32,33,34,37,38,39) +3V
(19,20,23,24,26,30,37) +5V

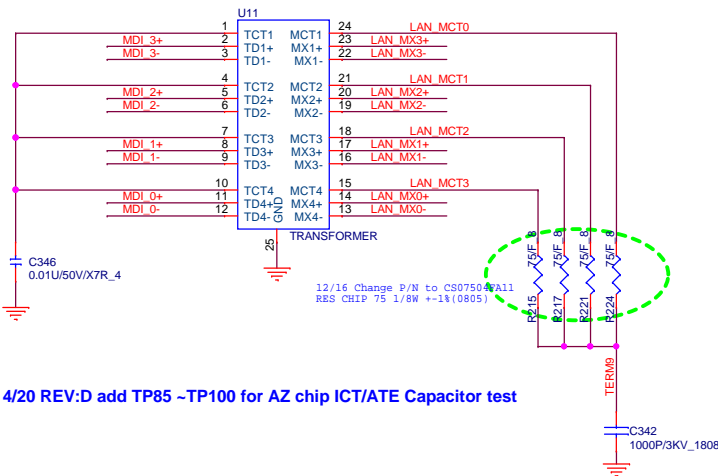


Leakage circuit (MPC)

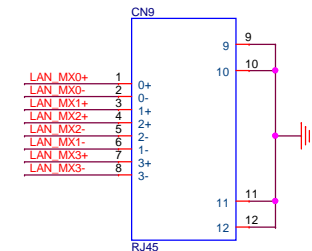


Transformer

Layout: All termination signal should have 30 mil trace

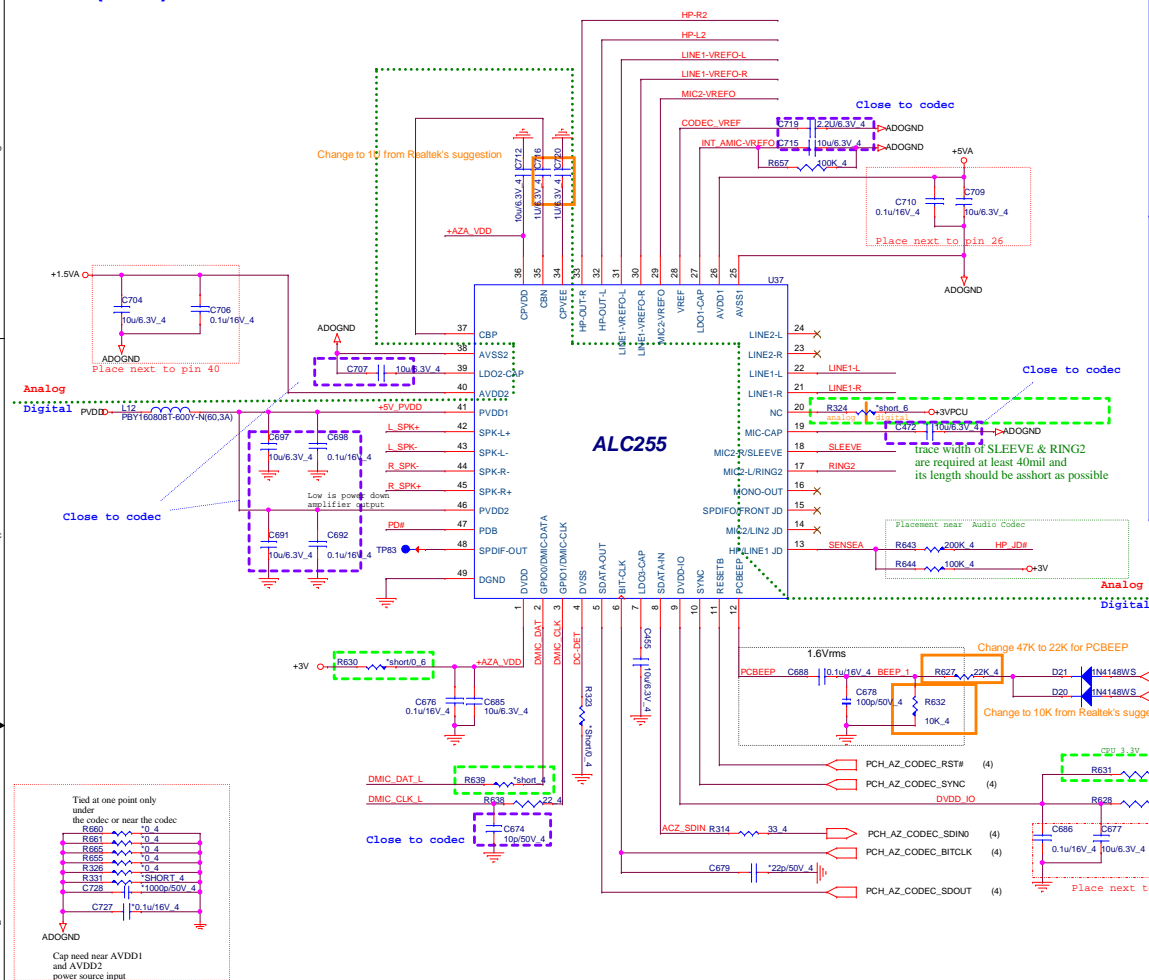


RJ45 Connector

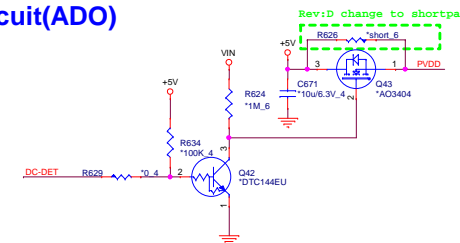


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PROJECT : ZRW

Codec(ADO)



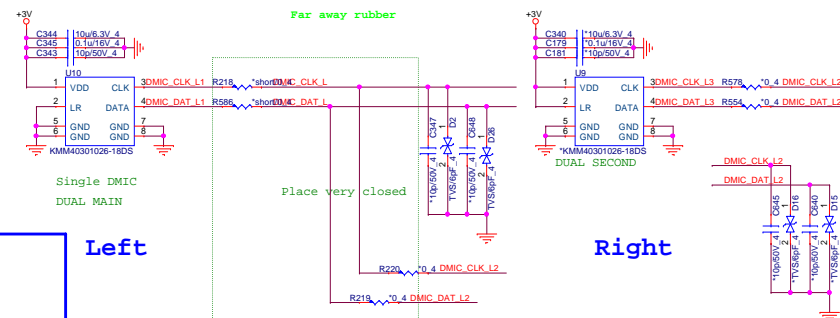
DC-DET circuit(ADO)



23

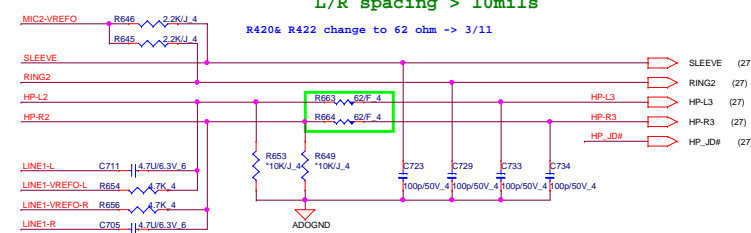
D-Mic (MIC)

Single DMIC and Dual DIMC same PN: AL403010A00

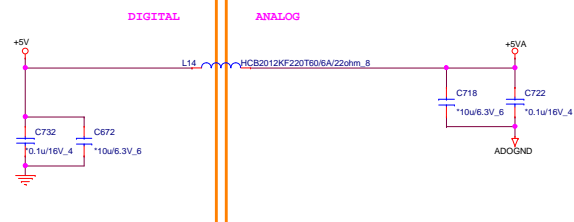


Universal Audio Jack HEADPHONE/MIC/LINE combo (ADO)

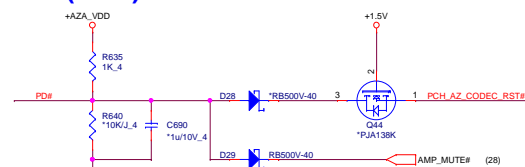
SLEEVE/RING2 trace > 40mils
HP/LINE trace > 10mils
L/R spacing > 10mils



Codec PWR 5V(ADO)

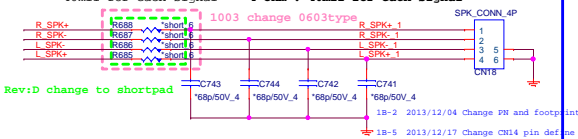


Mute(ADO)

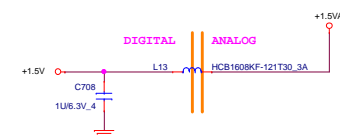


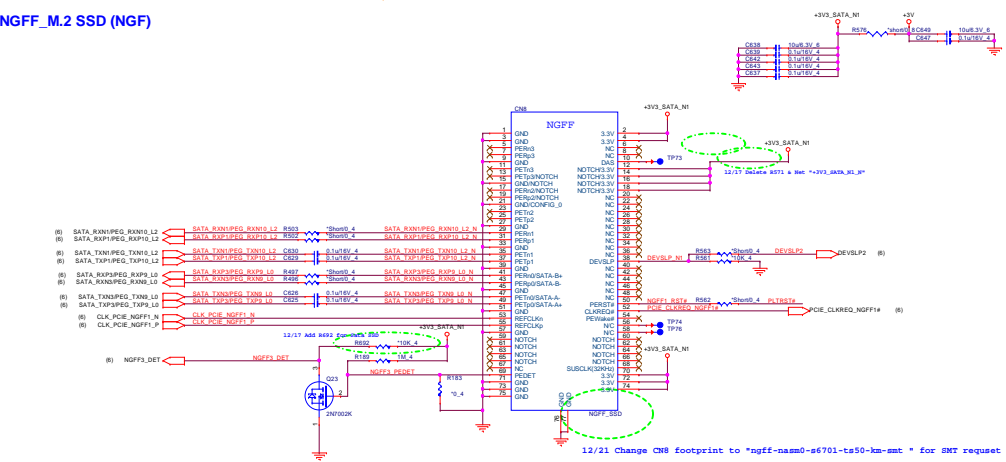
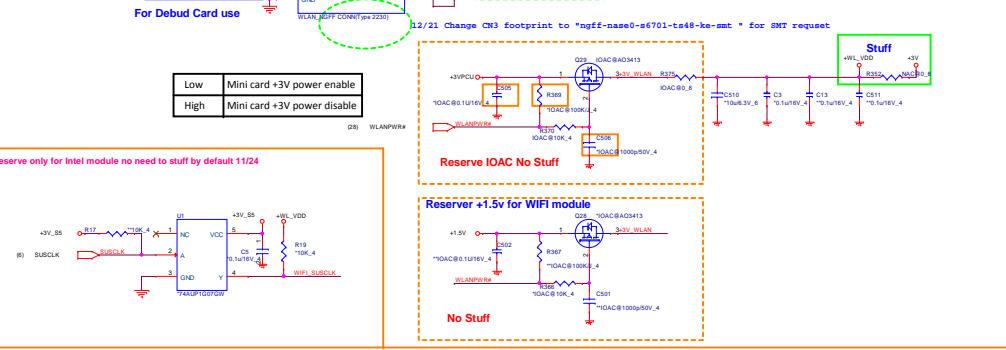
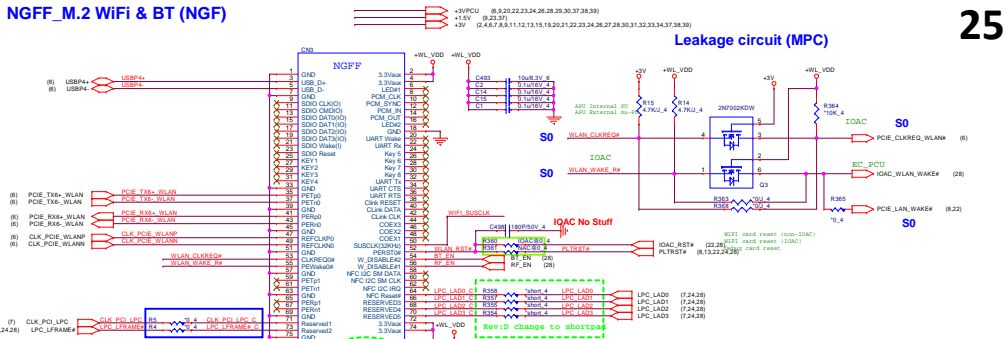
Internal Speaker

40mil for each signal 4 ohm : 40mil for each signal

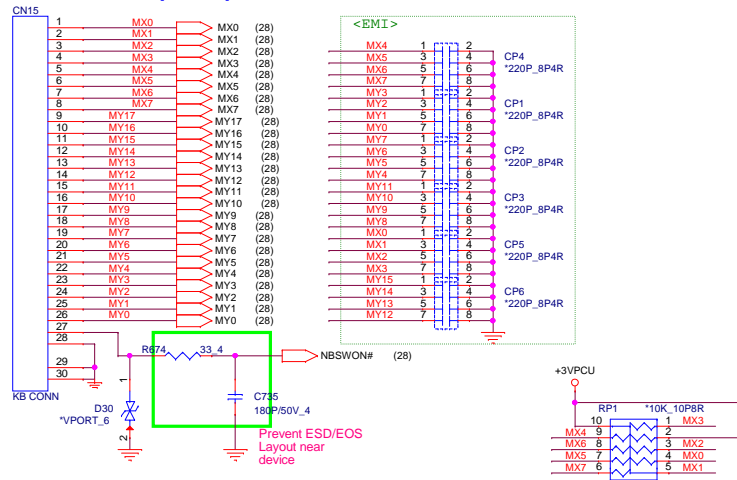


Codec PWR 1.5V(ADO)

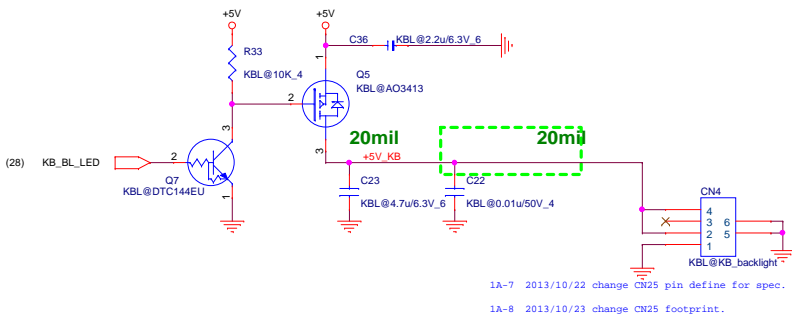




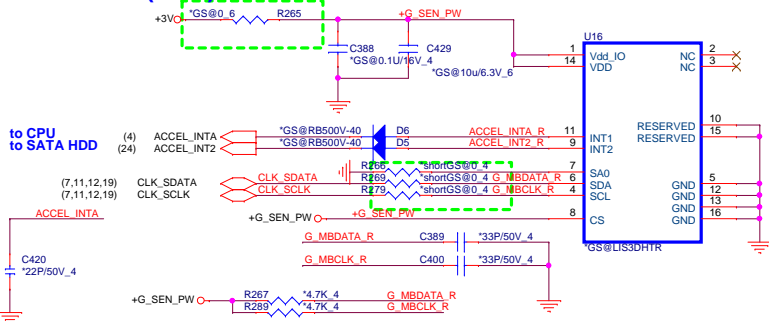
KEYBOARD (KBC)



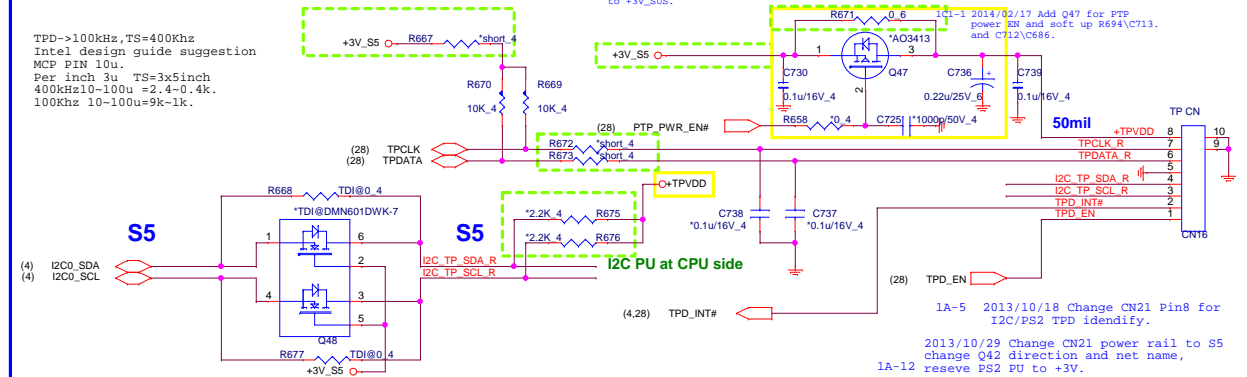
KB_LED (KBC)



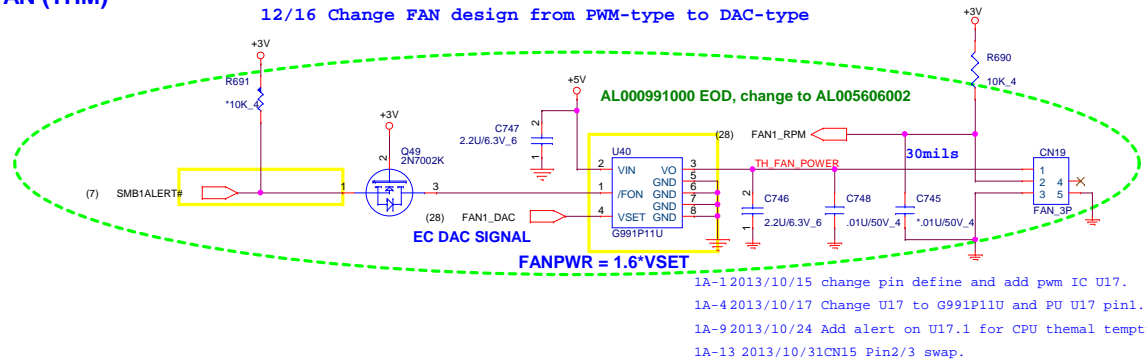
G-sensor(ACS)



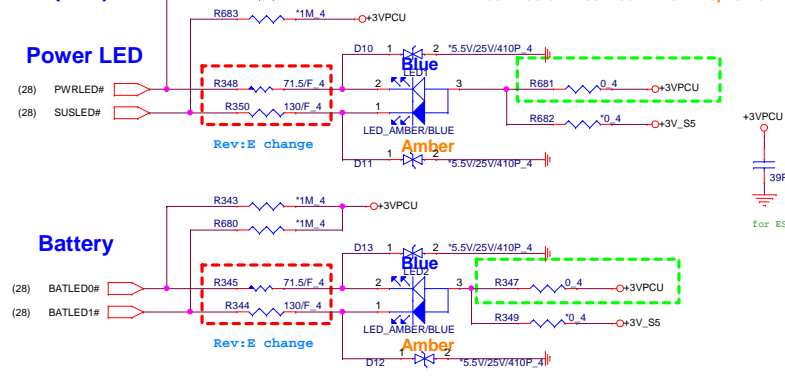
TOUCHPAD BOARD CONN (TPD I2C/PS2 co-lay)



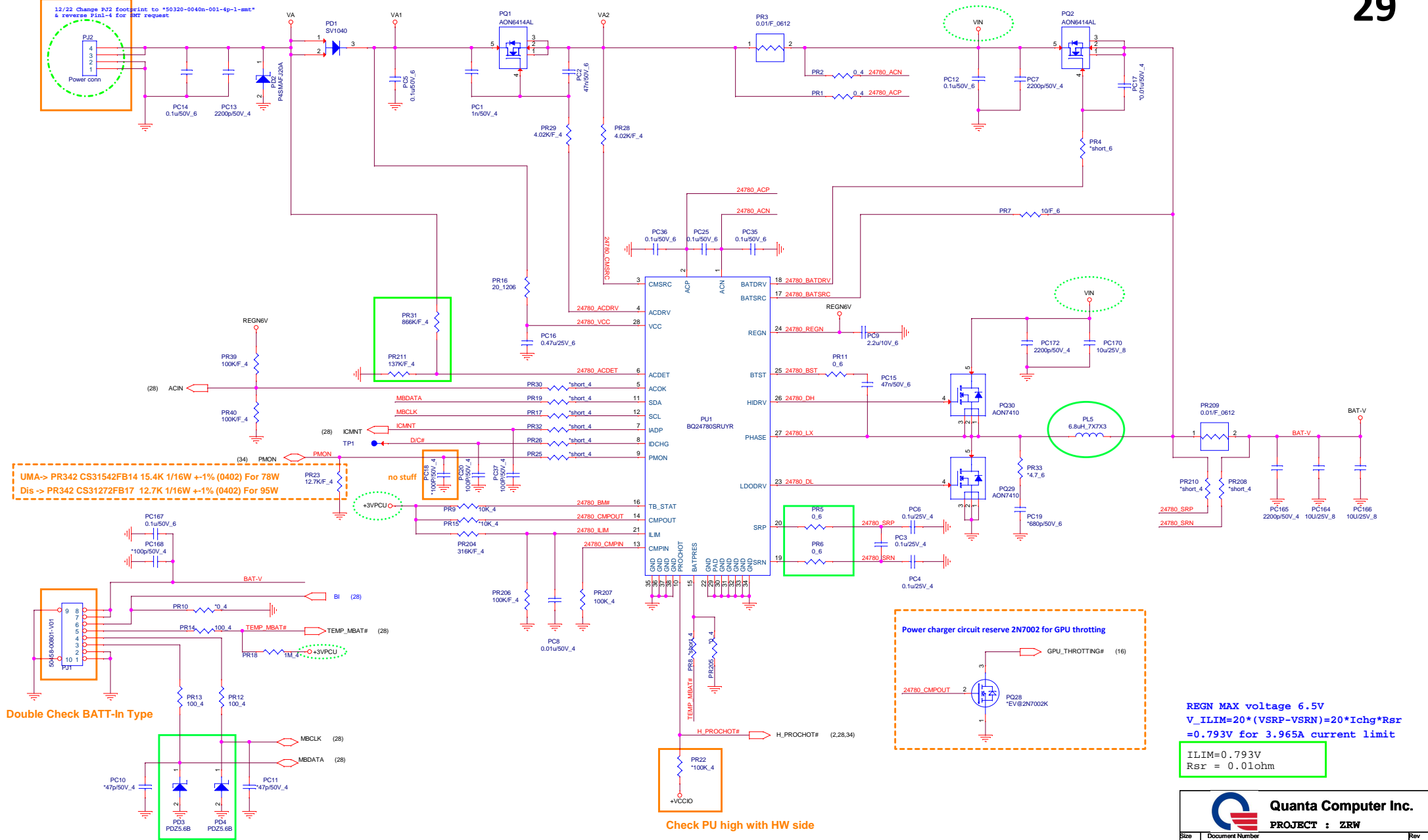
CPU FAN (THM)



POWER LED(UIF)

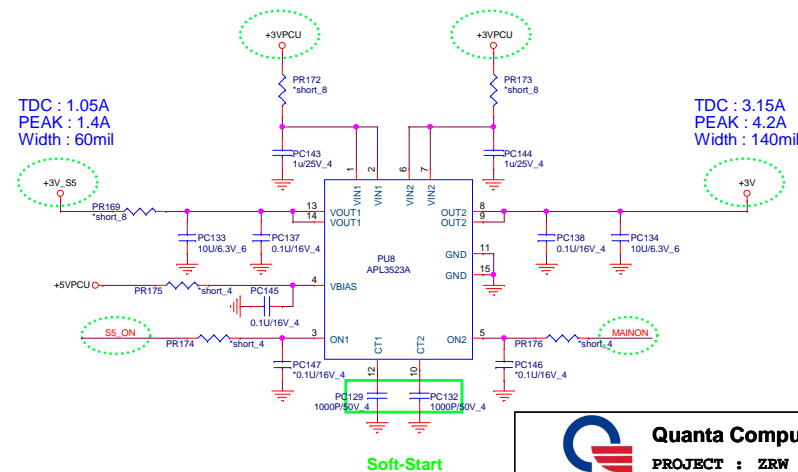
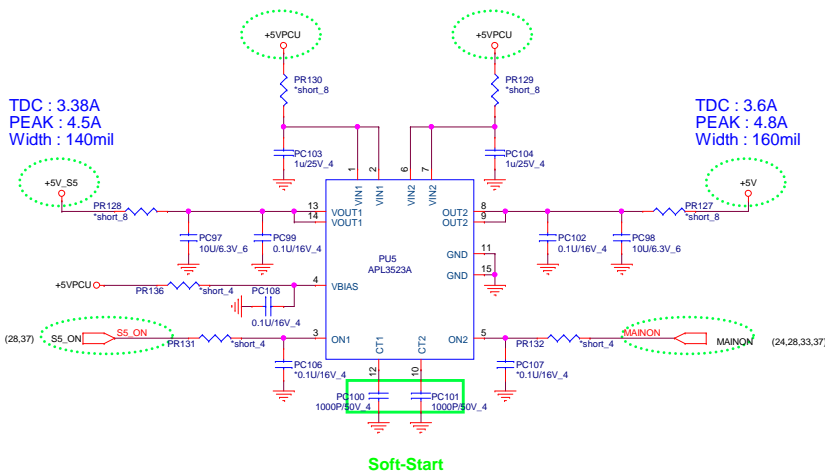
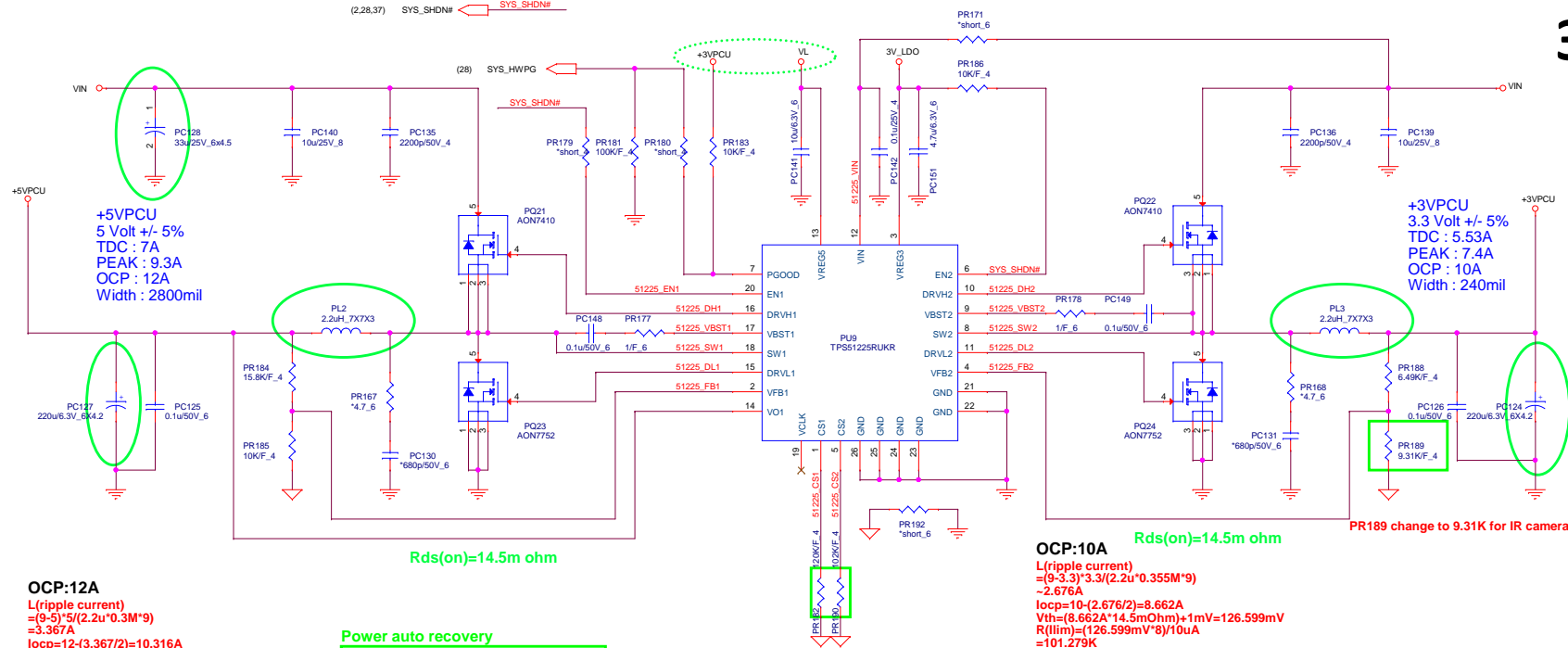


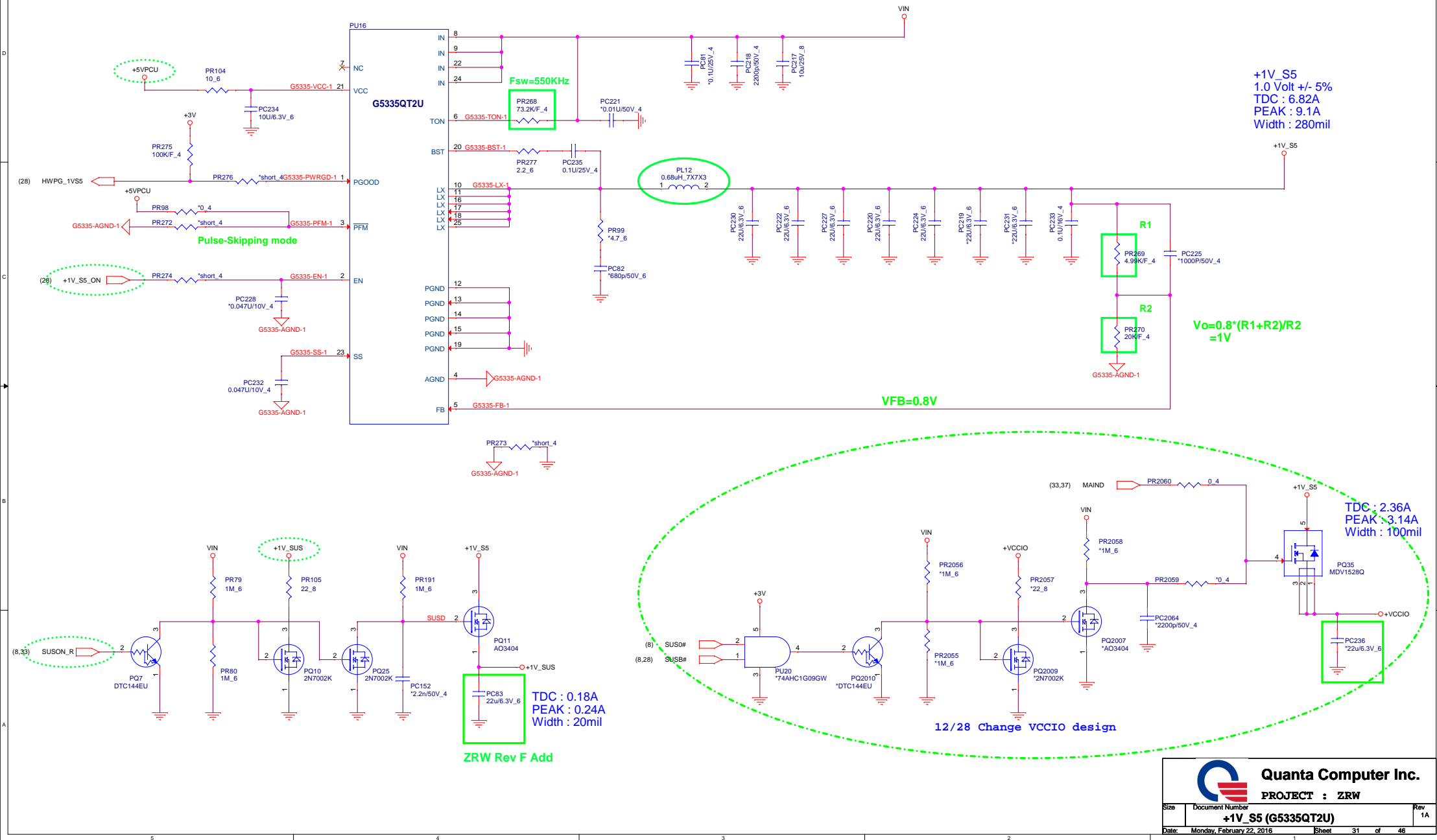
Double Check ADP-In Type



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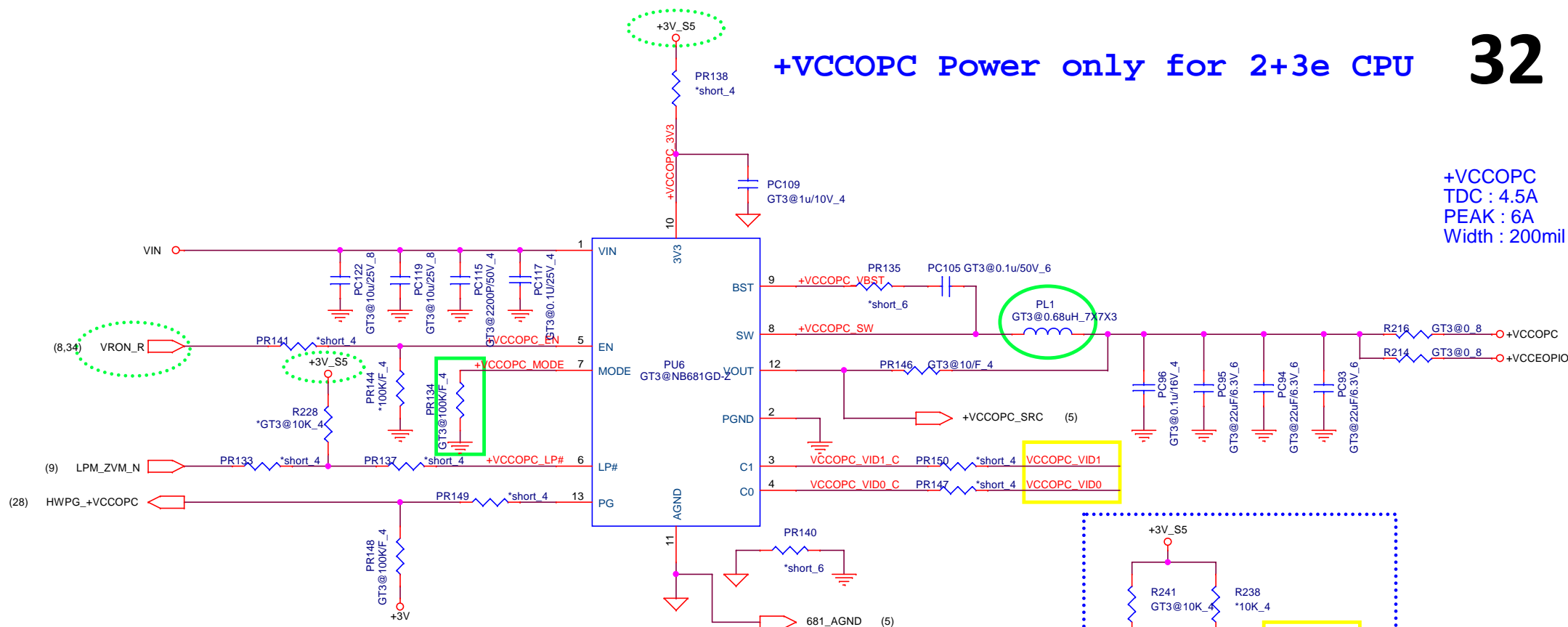
Size Document Number
Charger (BQ24780S)
Date: Monday, February 22, 2016 Sheet 29 of 46 Rev 1A





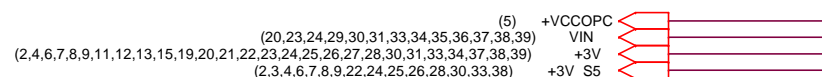
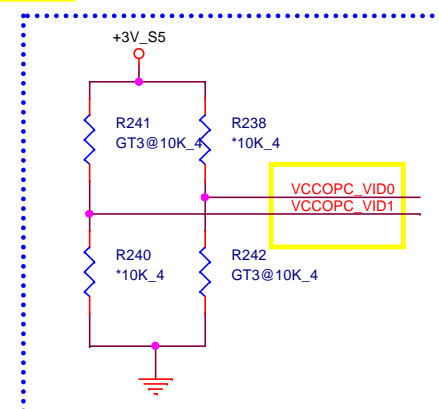
+VCCOPC Power only for 2+3e CPU

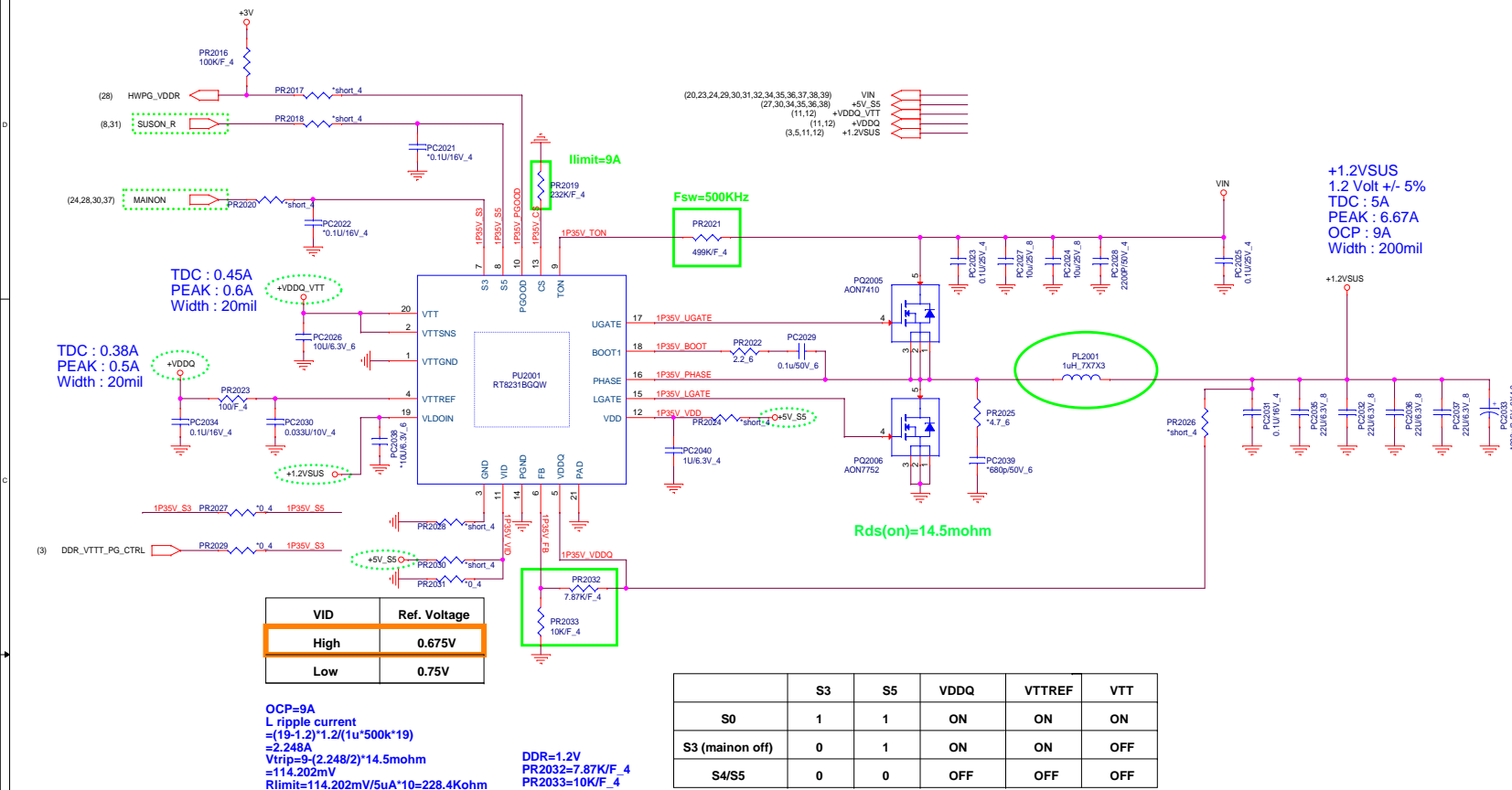
+VCCOPC
TDC : 4.5A
PEAK : 6A
Width : 200mil



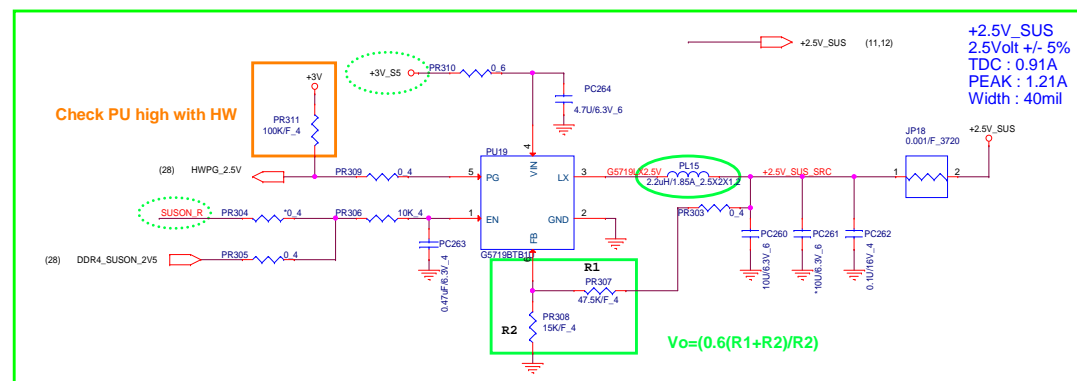
Mode	VR Rail
0 ohm	VCCIO
Floating	PRIMCORE
100K	EDRAM/EOPIO
150K	Other

	LP#	C1	C0	Vo
VCCEDRAM	0	X	X	0V
	1	0	0	0.8V(MSM
	1	0	1	0.95V
	1	1	0	1.0V
	1	1	1	1.05V

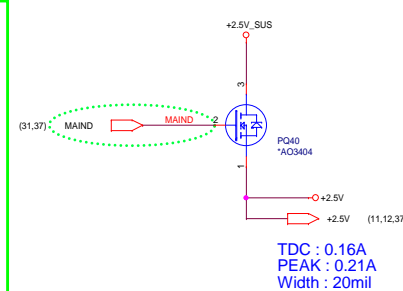




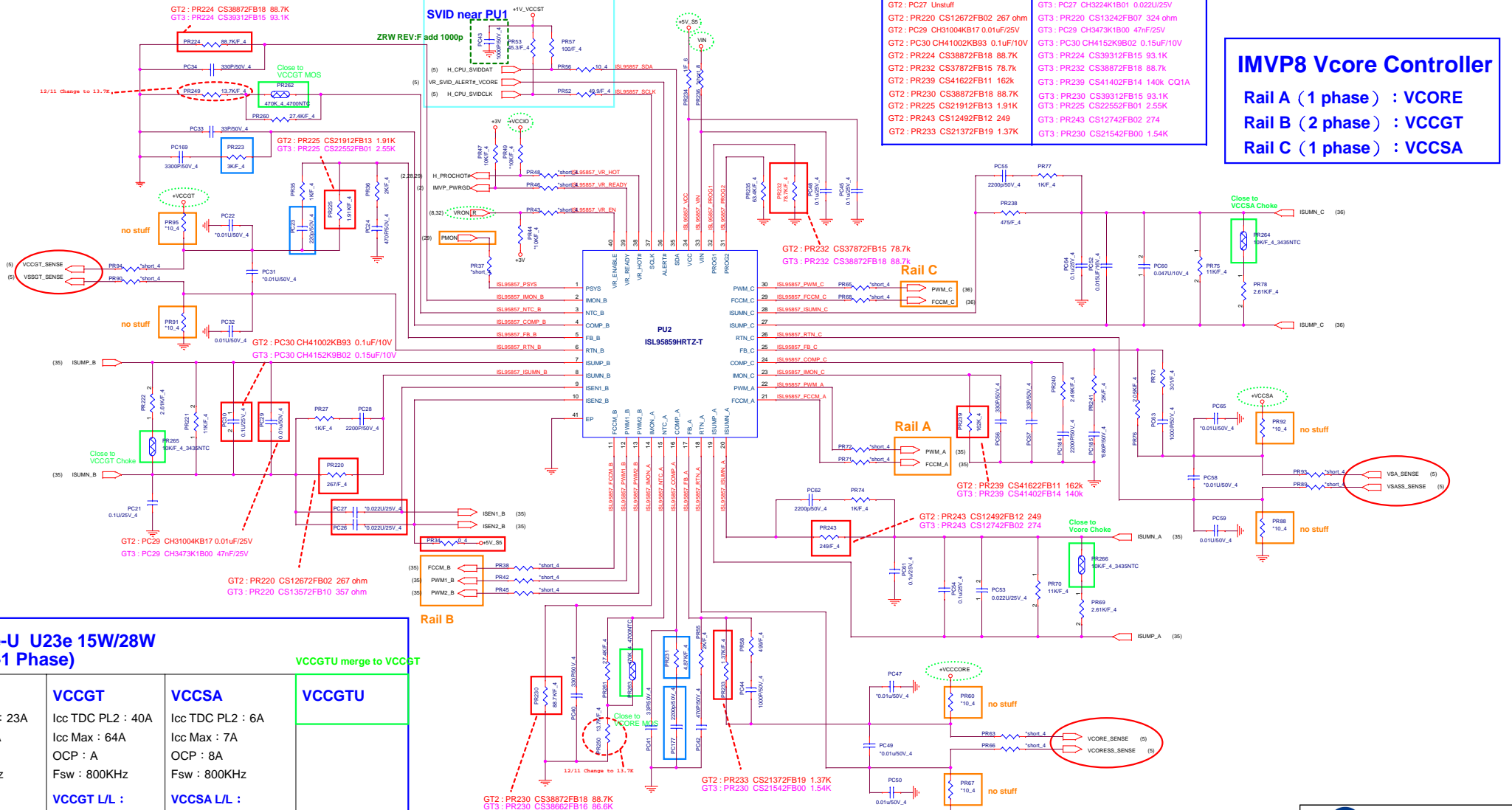
+2.5VSUS Power Rail For DDR4



10/26 Reserve +2.5V for DDR4 VDDSPD



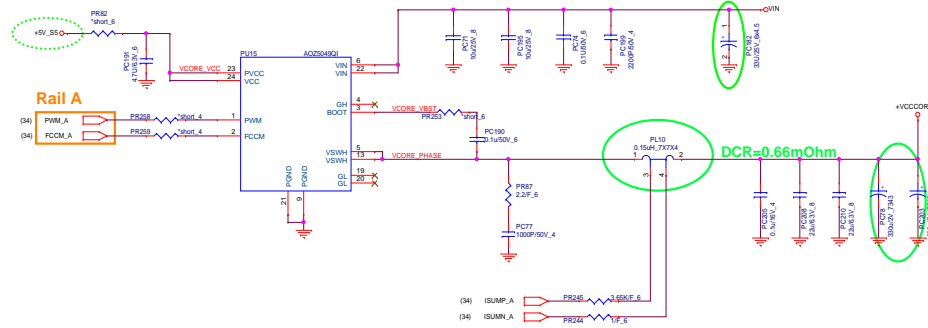
Check PU high with HW



GT2: PR19 Unstuff

GT3: PR19 CS41003F932 100K

VCORE



VCORE

Icc TDC PL2 : 23A

Icc Max : 29A

OCP : 35A

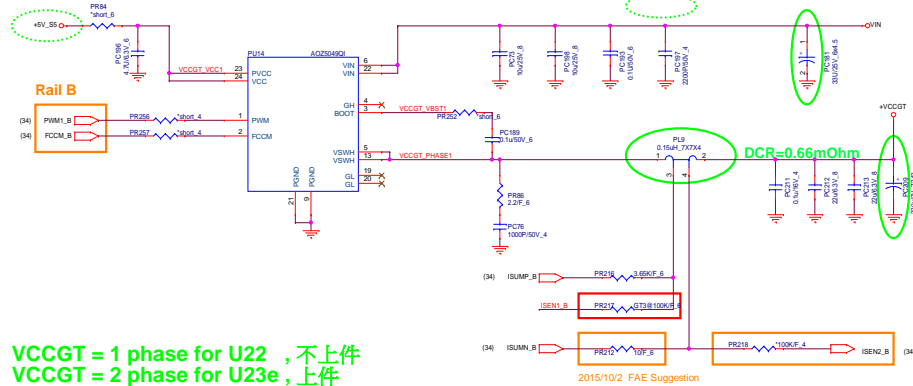
Fsw : 800KHz

VCORE L/L :

R_DC_LL : 2.1mV/A

R_AC_LL : 2.1mV/A

VCCGT



VCCGT

Icc TDC PL2 : 40A

Icc Max : 64A

OCP : A

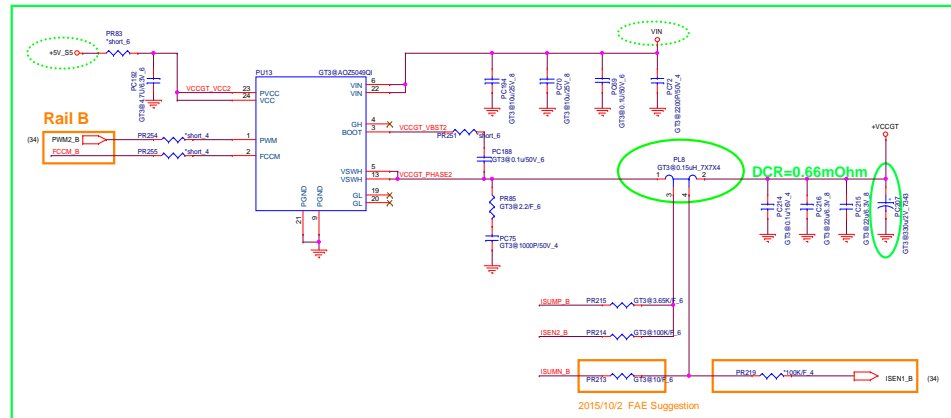
Fsw : 800KHz

VCCGT L/L :

R_DC_LL : 2mV/A

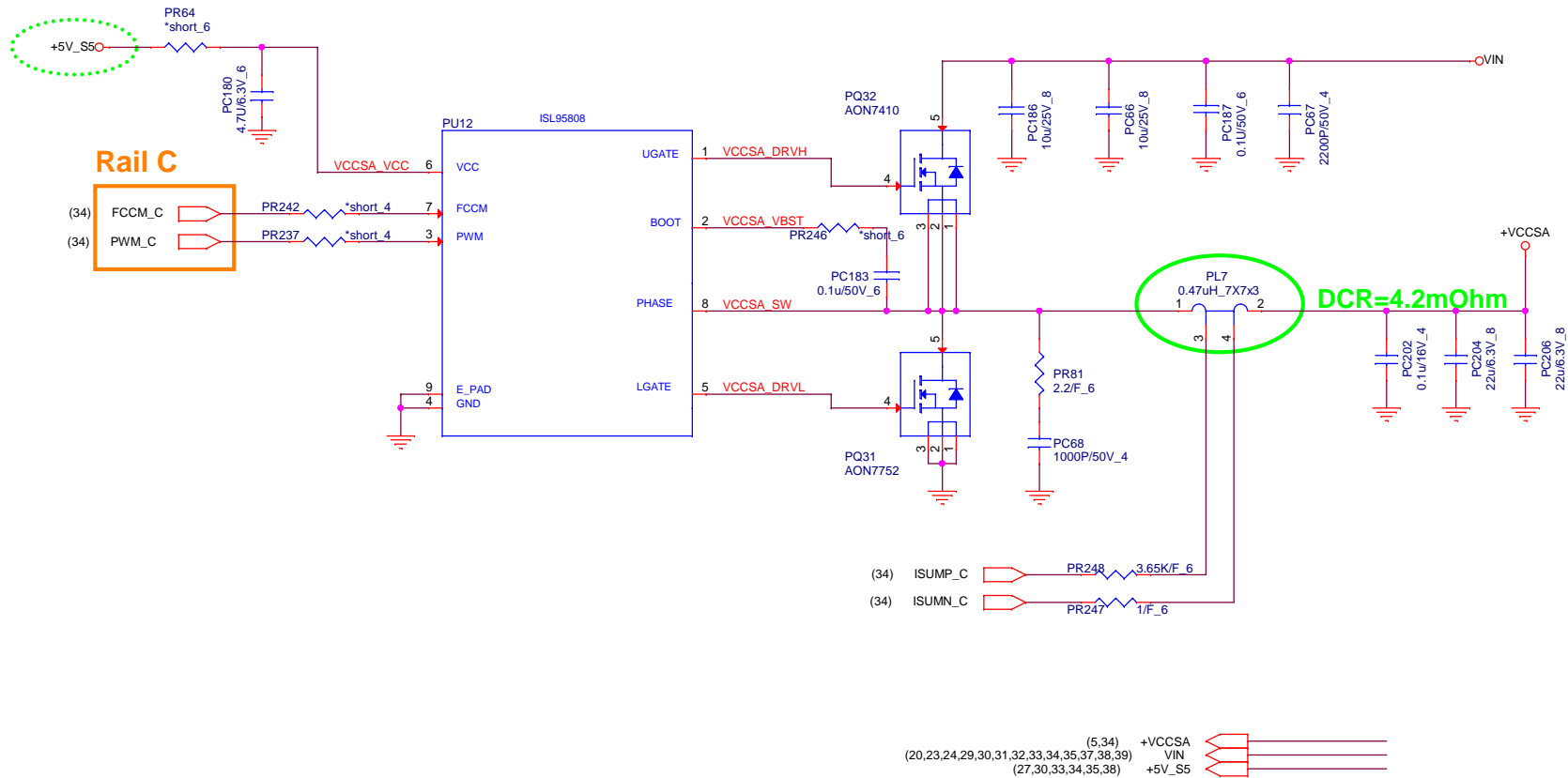
R_AC_LL : 2mV/A

VCCGT = 1 phase for U22 , 不上件
 VCCGT = 2 phase for U23e , 上件



(5,34) +VCCORE
 (20,23,24,29,30,31,32,33,34,36,37,38,39) VIN
 (5,34) +VCCGT
 (27,30,33,34,36,38) +5V_SS

VCCSA



VCCSA

Icc TDC PL2 : 5A

Icc Max : 5A

OCF : 6A

Fsw : 800KHz

VCCSA L/L :

R_DC_LL : 10.3mV/A

R_AC_LL : 10.3mV/A



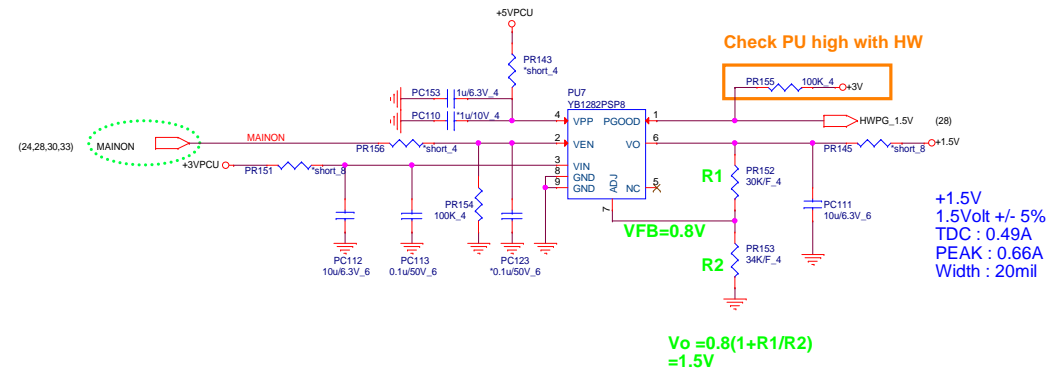
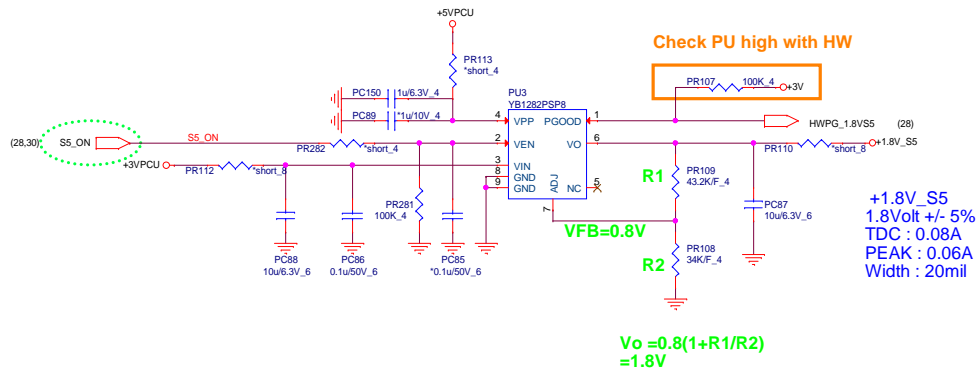
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PROJECT : ZRW

Size	Document Number	Rev
	VCCSA (ISL95808HRZ-T)	1A

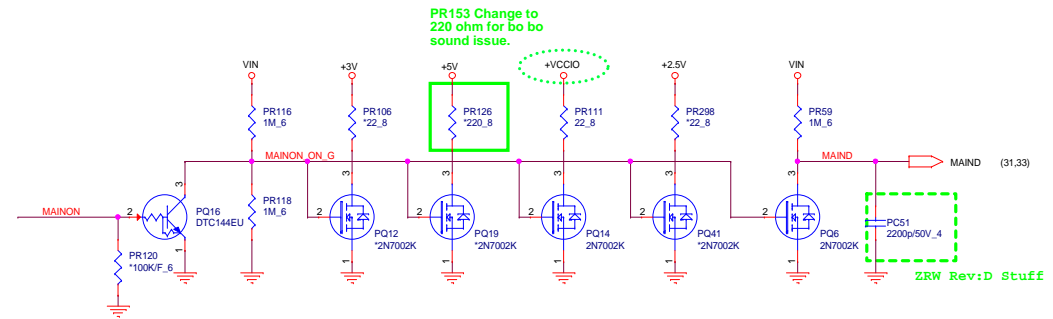
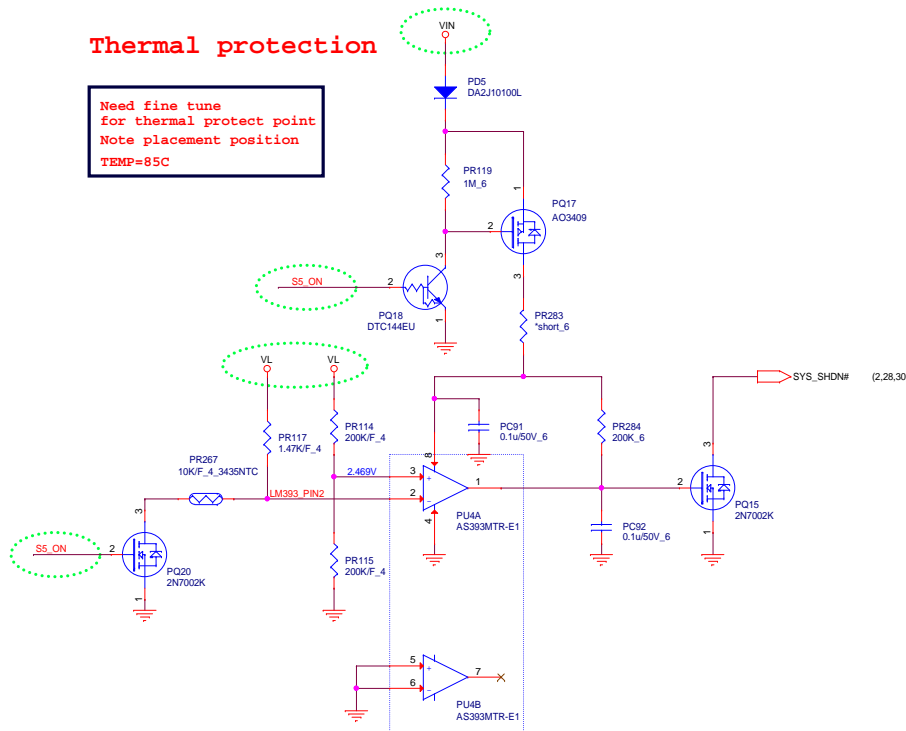
Date: Monday, February 22, 2016

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Thermal protection

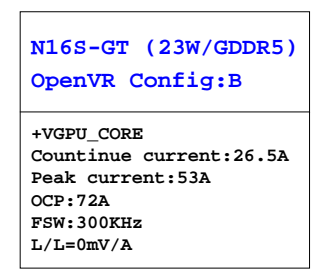
Need fine tune
for thermal protect point
Note placement position
TEMP=85C



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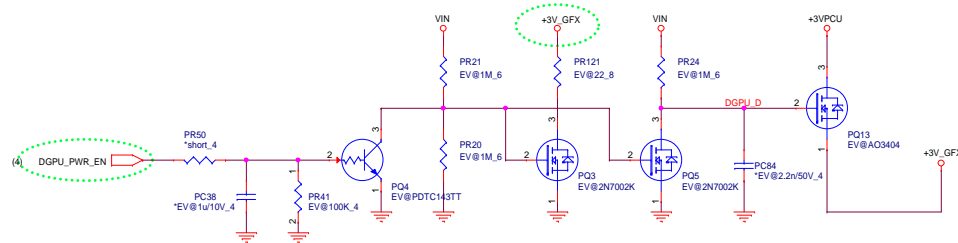
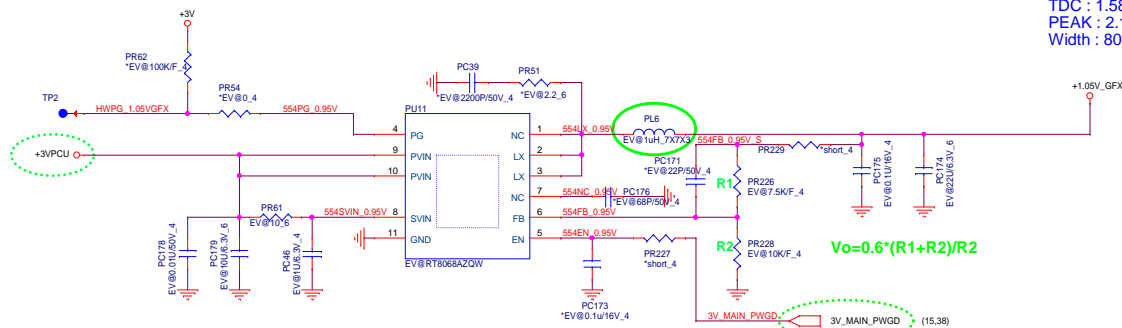
PROJECT : ZRW

Size	Document Number	Rev
	+1.8V/+1.5V/Thermal Protect	1A
Date:	Monday, February 22, 2016	Sheet 37 of 46



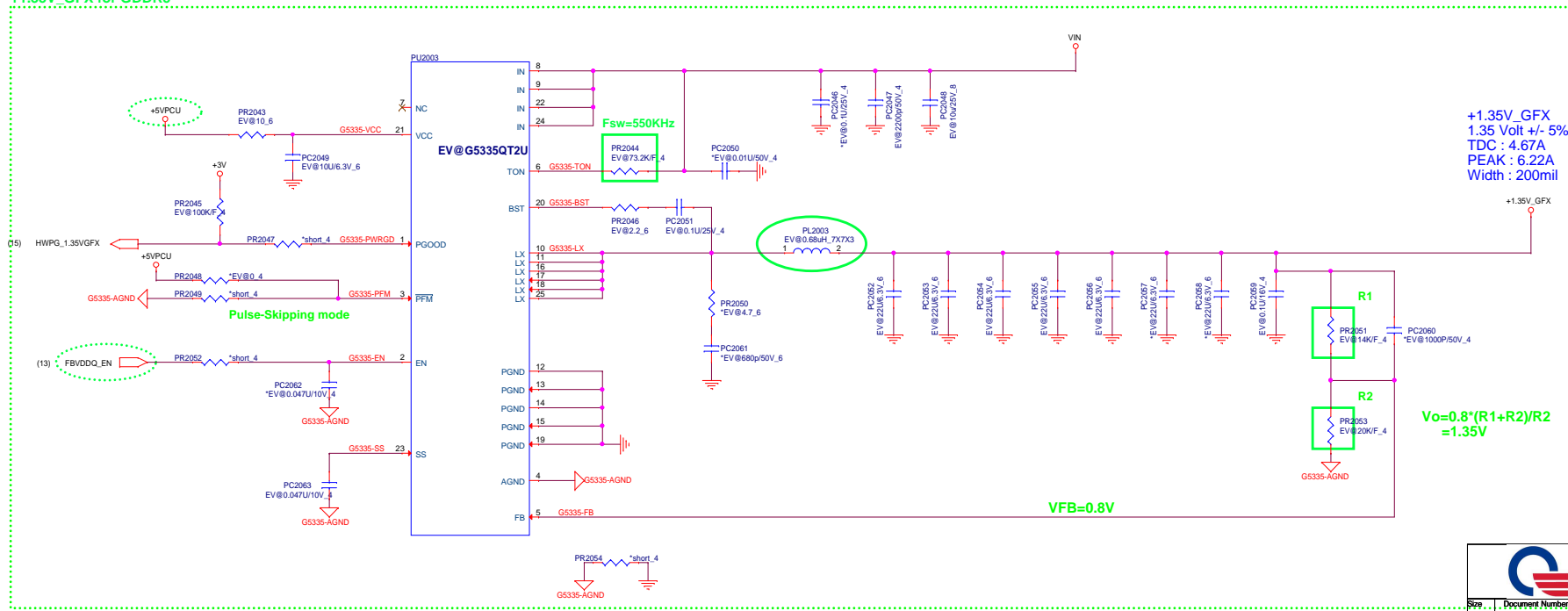
(13,14,15) +1.05V_GFX
(13,15,16,29) +3V_GFX
(14,16) +1.35V_GFX

+1.05V_GFX
TDC : 1.58A
PEAK : 2.1A
Width : 80mil



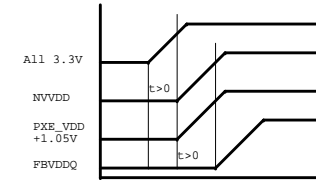
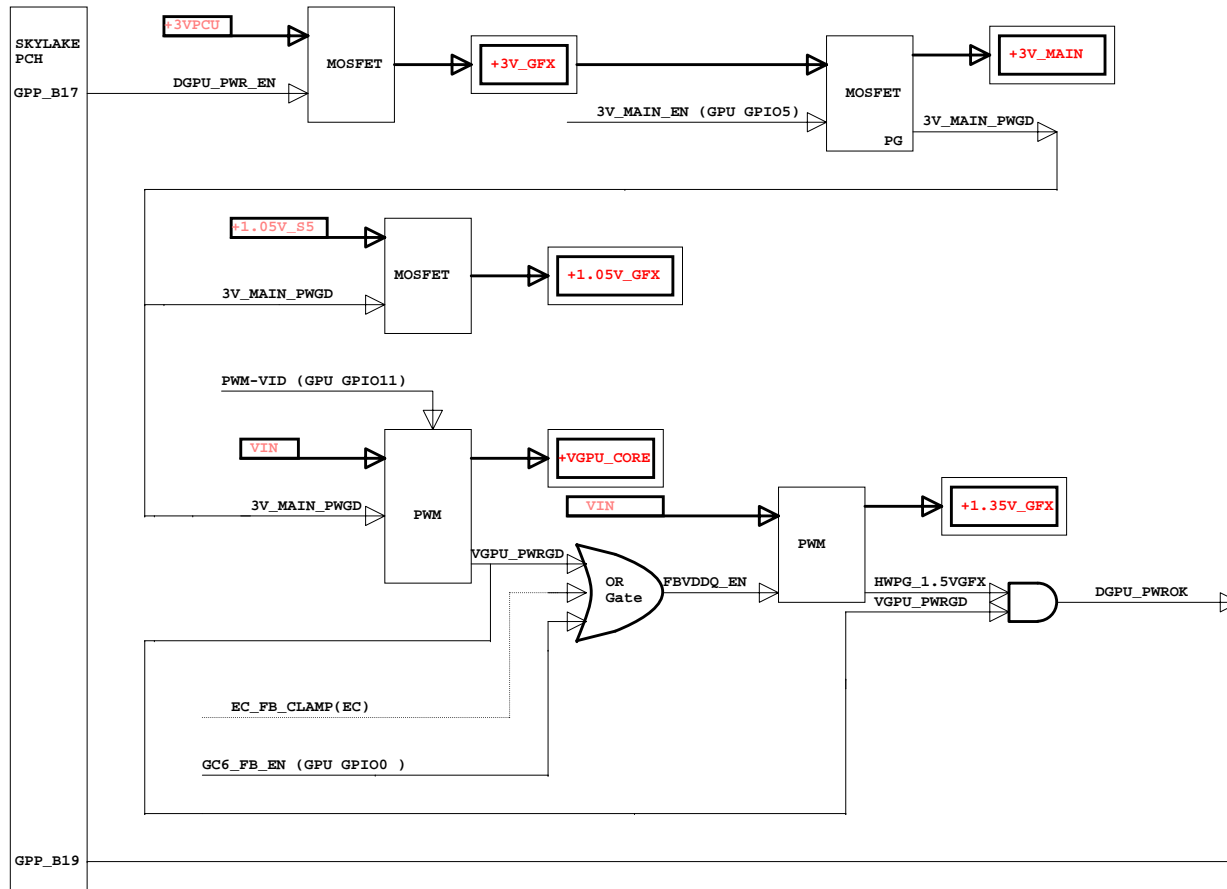
+3V_GFX
TDC : 0.05A
PEAK : 0.06A
Width : 20mil

+1.35V_GFX for GDDR5



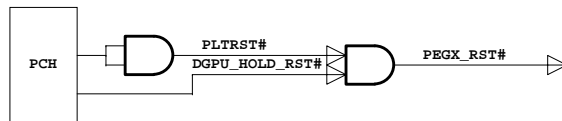
+1.35V_GFX
1.35 Volt +/- 5%
TDC : 4.67A
PEAK : 6.22A
Width : 200mil

VGA power up sequence

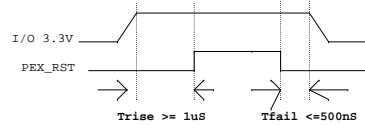


N15x Power on sequence
 Notes: -All 3.3V includes all rails powered at 3.3V
 -PEX_VDD 1.05V includes all rails that are shared

VGA Reset

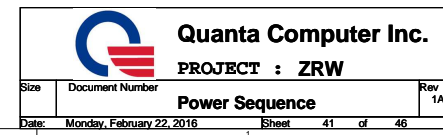


PEX_RST timing

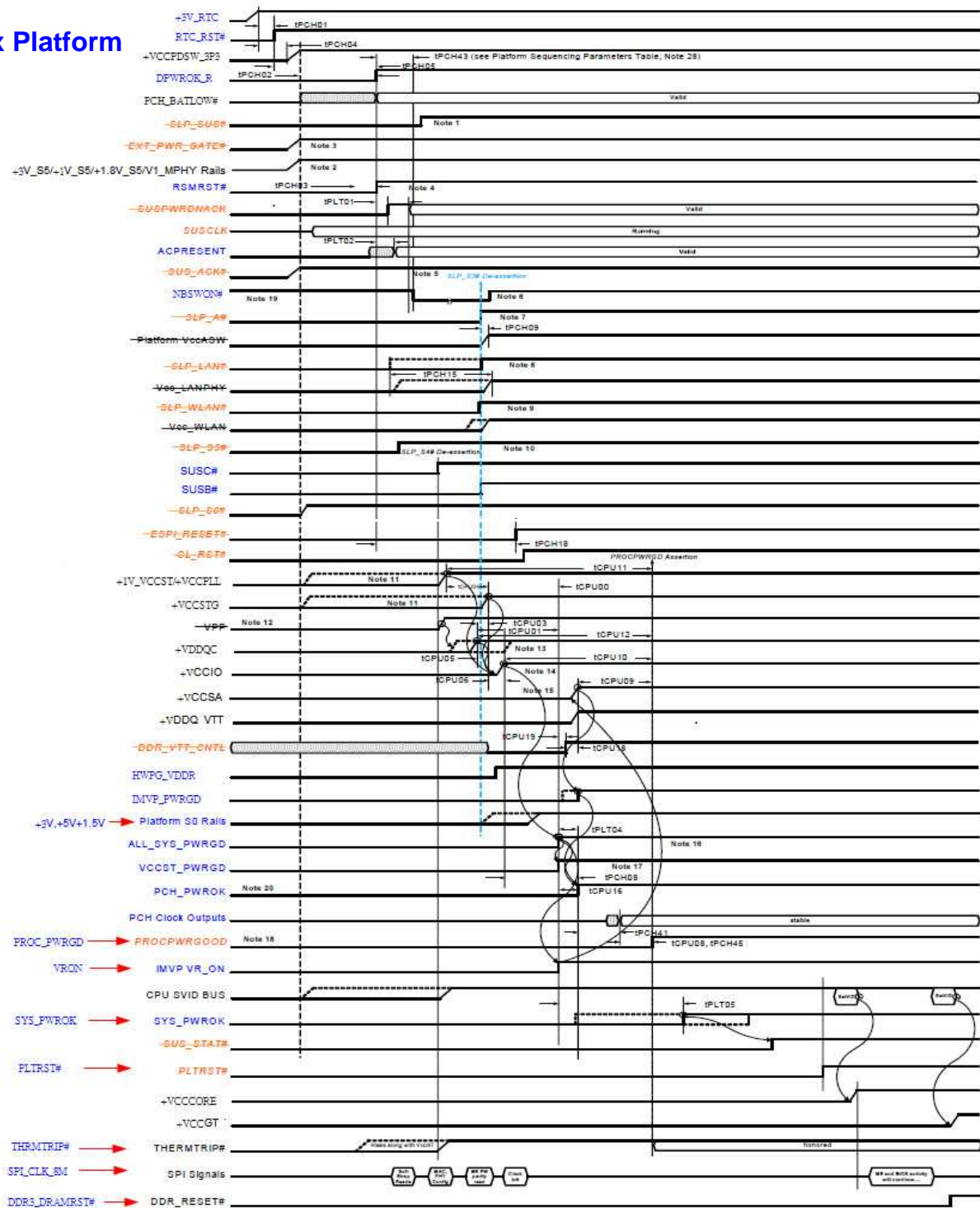


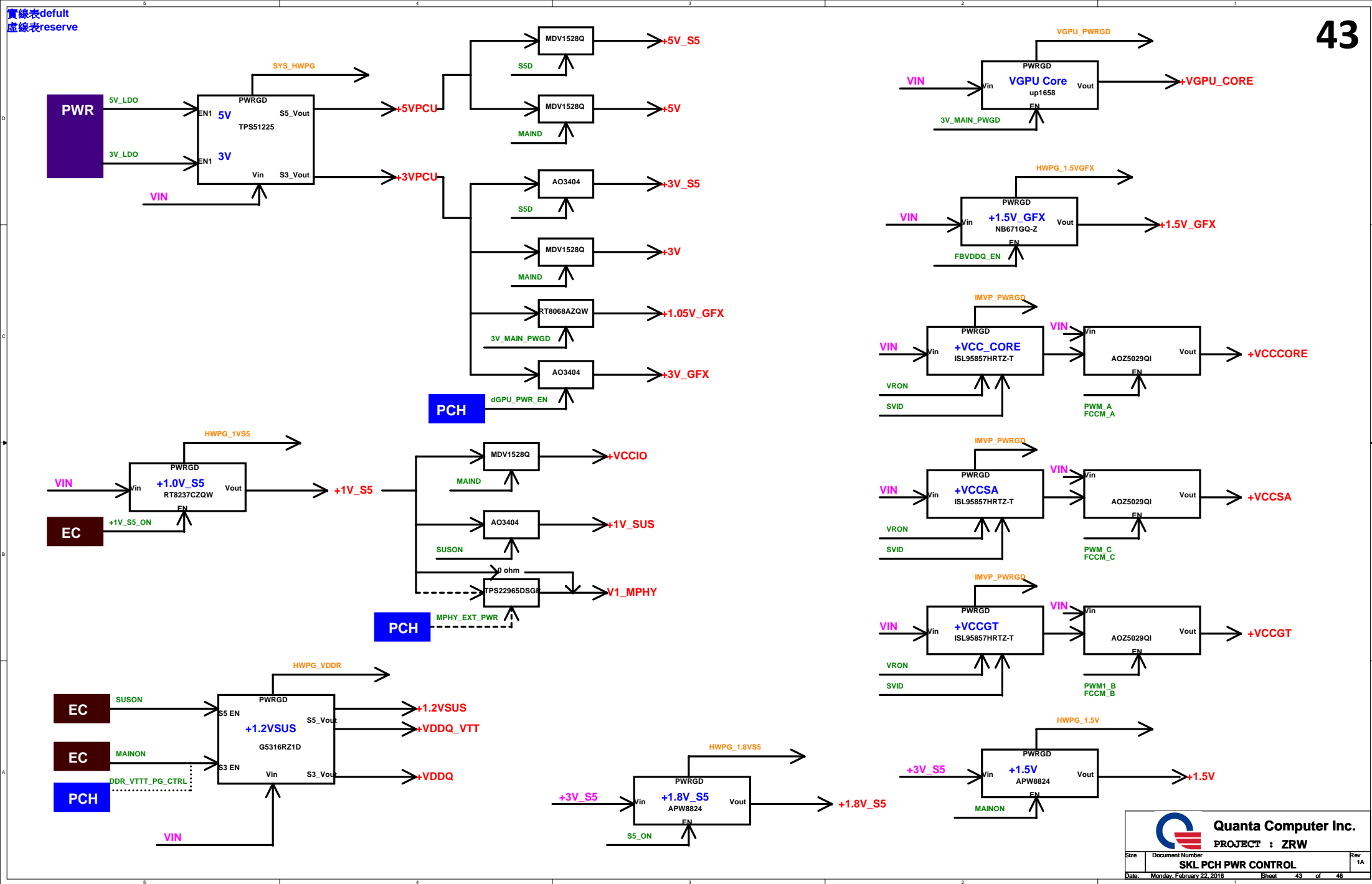
Non Deep Sx

41

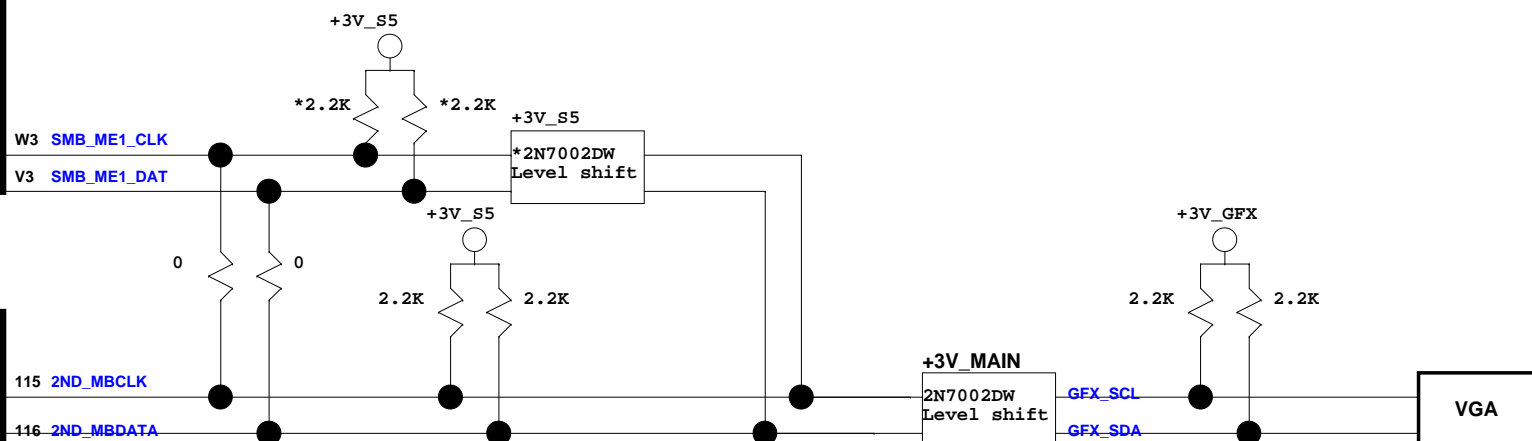
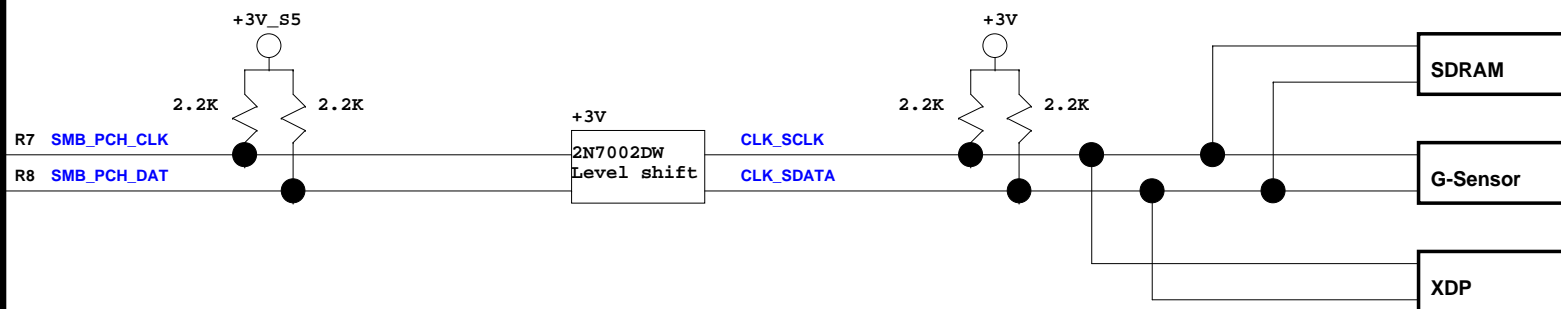


Skylake U Non-Deep Sx Platform Power on sequence





Skylake U

EC
IT8987CX